The ATM Forum
Technical Committee

Utopia Level 2, Version 1.0

af-phy-0039.000

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1. Introduction

1.1. Document Purpose and Background

This document describes a number of enhancements to the *Universal Test & Operations PHY Interface for ATM* (UTOPIA) data path interface [1]. This document assumes familiarity with the Level 1 Utopia document [1], which specifies the following :

1. an 8-bit wide data path, using an octet-level handshake, operating up to 25 MHz, with a single PHY device

2. an 8-bit wide data path, using an cell-level handshake, operating up to 25 MHz, with a single PHY device

3. a cell format and extra signals for a 16-bit wide data path for future use

The Level 1 Specification was designed to deal with the following PHY layer interfaces :

1. 155.52 Mbps (SONET/OC-3c)
2. 155.52 Mbps (8B/10B block coded)
3. 100 Mbps (4B/5B TAXI)
4. 44.1236 Mbps (DS-3)
5. 51.84 Mbps (OC-1)

We recommend use of this document in conjunction with the Level 1 Specification, since only updates and changes to it are described here.

1.2. Scope

Various levels of the Utopia specification will document enhancements to the Level 1 specification. Level 2, described in this document addresses the following areas :

1.2.1. Definition of AC and DC Characteristics

The description on AC characteristics features three different clock rates :

a) 25 MHz : Better definition of the timing at this speed.

b) 33 MHz data path interface operation, intended to simplify PCI Bus ATM layer designs. This clock rate is used both with 8 and 16-bit wide data paths. The 16-bit wide data path uses the cell format and signals described in the Level 1 document.

c) 50 MHz data path interface operation, intended for a 16-bit interface at line rates of 622 Mbps.

1.2.2. Multi-PHY (MPHY) Operation

This will define the "physical" operation of up to n PHY devices where,
n =< 8 at ATM layers intended for 155 Mbps;
n =< 4 at ATM layers intended for 622 Mbps.

with the virtual space set up for n =< 31.

1.2.3. Amended Level 1 Specification

The description of the Transmit and Receive interfaces in the Level 1 specification is clarified by the text described here. Thus, chapter 3 of this document is an update to chapters 4 and 5 of the Level 1 specification. There are no material or functional changes in the specification; the amended specification described here is intended solely to aid developers by providing a richer set of examples and a better description of the protocol.

1.3. Statement of Compatibility with Level 1 Document

Compatibility of the MPHY enhancement with the Level 1 specification is defined in the following terms :

1. **Downward Compatibility with Level 1** defines the operation of devices from all future Utopia Levels without glue logic in a Level 1 environment.

2. **Upward Compatibility for Level 1** defines the operation of Level 1 devices in Level 2 and future environments, with minimal glue logic.

1.4. Document Contents

This document focuses on the following aspects of Utopia :

1. Enhancements to the data path transfer protocols described in the Level 1 document. Thus, the document assumes use in conjunction with the Level 1 document, and minimizes repetition between the two documents.

2. Additional signal definitions to address the new data path functionality.

3. Detailed AC and DC characteristics

4. Amended Specification for parts of chapters 4 and 5 from the Level 1 Document.

2. Functional Description

2.1 Conventions

Identical to the Level 1 Specification.

2.2. Terminology related to Utopia Scope

The terminology here defines Utopia functionality that is addressed as part of Level 2 as well as some aspects that could potentially be addressed in future Utopia releases.

2.2.1. Higher Speed on Parallel Interface

A speed of 33 MHz is intended to run on both 8-bit and 16-bit wide buses, and is designed for PCI. A speed of 50 MHz is also described by this document.

2.2.2. Wider Data Path

A 16-bit datapath is intended for 622 Mbps operation with a speed of 50 MHz or higher on the parallel bus.

2.2.3. Multi-PHY Operation

This will define the "physical" operation of up to n PHY devices where,

n =< 8 at ATM layers intended for 155 Mbps;
n =< 4 at ATM layers intended for 622 Mbps.

with the virtual space set up for n =< 31. This allows for up to 31 ports on up to 8 PHY devices.

2.2.4. Management Interface

The Level 1 specification shows an interface used by an management entity to configure, manage, and monitor one or more PHY devices. The definition of this interface will include :

a) configuration/features - both commands and status
b) interface
c) protocol : in or out of band
d) timing

Utopia Level 2 describes a management interface in an informative appendix.

2.2.5. Board-Board Interface

A timing specification for longer distances, such as a backplane or a mezzanine bus. This functionality is not part of Utopia Level 2 and is for further study.

2.2.6. Downward Compatibility with Level 1

This defines the operation of devices from all future Utopia Levels without glue in a Level 1 environment.

2.2.7. Upward Compatibility for Level 1

This defines the operation of Level 1 devices in Level 2 and future environments, with minimal glue logic.

2.2.8. Multi-ATM with Multi-PHY

This will define operation of up to m ATM devices and n PHY devices where,
m + n =< 10 at ATM layers intended for 155 Mbps;
m + n =< 6 at ATM layers intended for 622 Mbps.

The definition will consider issues of :
a) dynamic allocation
b) goodput
c) fairness
d) redundancy
e) flow control

This functionality is not part of Utopia Level 2 and is for further study.

2.2.9. Serial Interface

A Utopia Interface with less than or equal to X pins, where X = approximately 2. E.g. P1355. This functionality is not part of Utopia Level 2 and is for further study.

2.2.10. Inter-Rack Communication

A method for communication across racks. This functionality is not part of Utopia Level 2 and is for further study.

2.2.11. GFC Support

Support for the GFC field. Areas of study related to Utopia include :

a) new signal for ABR counter reset : a better description of this may be provided in a later version of Utopia based on common use of the GFC field
b) new signal for halt on both receive and transmit
c) minimum latency on above function

This functionality is not part of Utopia Level 2 and is for further study.

2.2.12. Low Latency Mode

A low latency mode for the Utopia Interface. This functionality is not part of Utopia Level 2 and is for further study.

2.2.13. Mechanics

Board Profiles and Connectors, which are not part of Utopia Level 2 and are for further study.

2.2.14. Test Interface

A separate interface for test purposes. This functionality is not part of Utopia Level 2 and is for further study.

2.3. Other Terminology

2.3.1. MPHY Device

A PHY layer device that supports the MPHY interface on Utopia, which may consist of one or more PHY ports.

2.3.2. MPHY Port

A PHY layer port has a one-one correspondence with one Physical Media Dependent (PMD) entity.

2.3. Reference Model and Configurations

The basic reference model for Utopia is represented by Figure 2.1. This describes functionality for one ATM layer connected to one PHY layer, with an associated management entity. Figure 2.2 depicts an extended reference model. Both figures show that, for now, the scope of Utopia is limited to the interface between the ATM and PHY layers. Figure 2.3 depicts various Utopia reference configurations based on the reference model. The Level 2 specification is intended to address the reference configuration shown in Figure 2.3b.

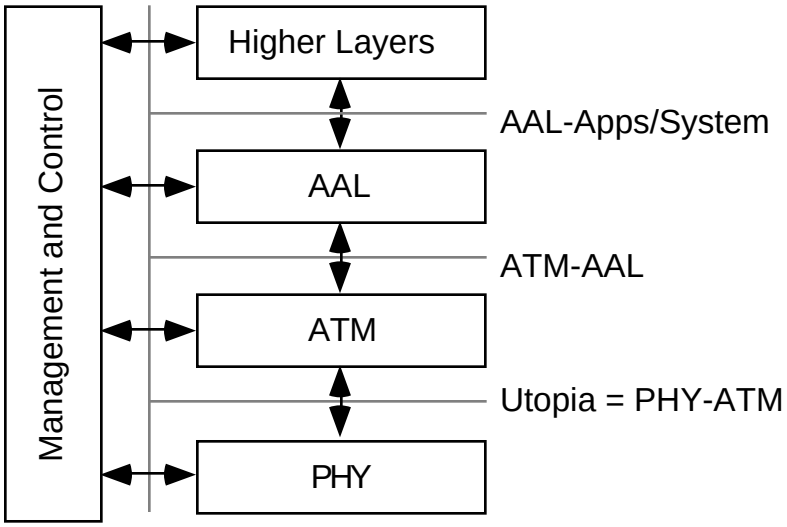


Figure 2.1. Basic Reference Model

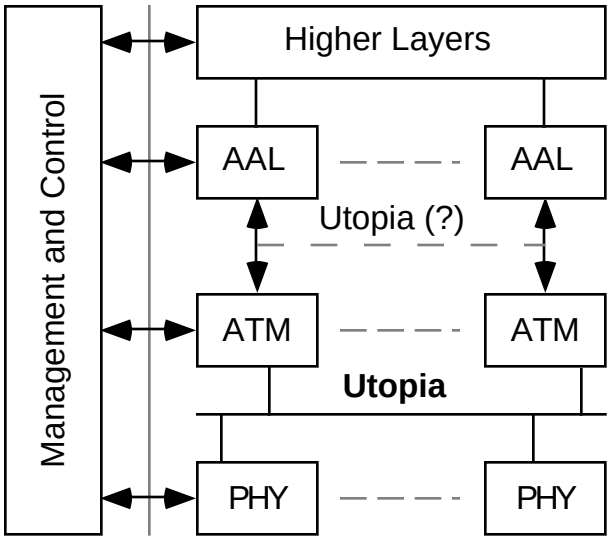


Figure 2.2. Extended Reference Model

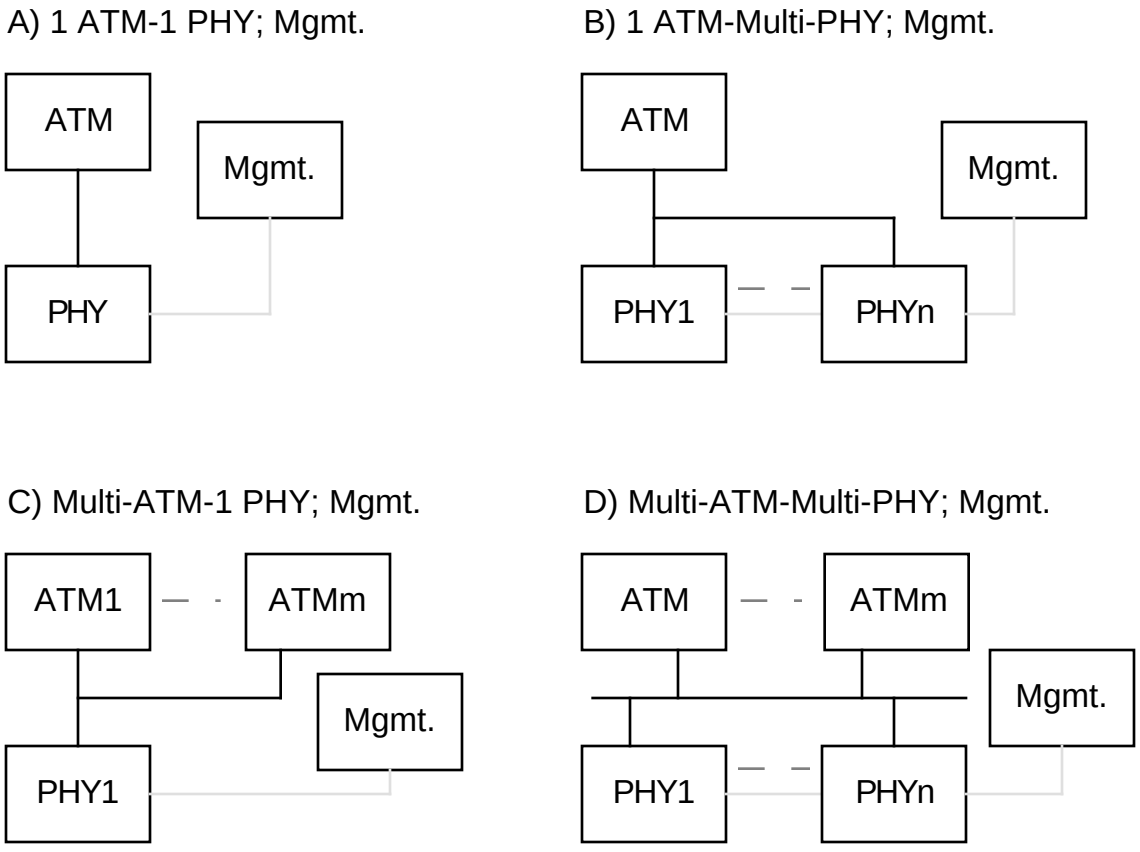


Figure 2.3. Reference Configuration

2.4. Interface Rates

Transmit and Receive transfers are synchronized via their respective interface transfer clock. No changes to the Level 1 specification, except for the formal addition of 622 Mbps (OC-12, and OC-12c) on a 16-bit data path.

2.5. Device Capabilities

Synchronization, rate matching, the cell format in 8-bit mode, and signal relationships to the enable and start of cell signals do not change with respect to the Level 1 specification. 8-bit mode is recommended for all line rates up to 155 Mbps, with 16-bit mode recommended for use with a line rate of 622 Mbps, and a parallel interface running at up to 50 MHz.

2.6. Cell Processing

The cell transfer format for 8 and 16-bit modes is described in the Level 1 specification and is unchanged. The cell transfer format for 16-bit mode, which is also described in the Level 1 specification, is shown in Figure 2.4 for reference.

In 16-bit mode, 54-octet cells are transferred between ATM and PHY layers. As for 8-bit mode, a user-defined field is provided for backward compatibility. The byte arrangement is Big-Endian.

Bit 15	Bit 0	(16 Bit Mode)
Header 1	Header 2	
Header 3	Header 4	
UDF1	UDF2	UDF = User Defined (e.g. HEC)
Payload 1	Payload 2	
:	:	|
:	:	time
:	:	|
Payload 47	Payload 48	V

Figure 2.4. Cell Format in 16-bit mode

If the UDF field is utilized for the HEC, it is recommended that the HEC octet is carried in the UDF1 field. The UDF2 field maybe used to provide control over the HEC for test purposes[1]. The field is also provided for backward compatibility to existing devices. Utopia considers HEC functionality to be part of the PHY layer.

[1]This field allows either/both ATM/SAR to implement HEC, and can provide Header Control/Status functions.

3. Amended Level 1 Specification

3.1. Introduction and Motivation

The purpose of this section is to clarify some aspects of the transmit and receive protocols in the Level 1 specification. There are no material changes to the operation of the interface; in particular, the text described here does not imply any implementation changes to devices based upon the Level 1 Specification.

This section addresses chapters 4 (transmit interface) and 5 (receive interface) of the Level 1 document only. Each chapter has two sections :

1. Signals, which is unchanged except to state that the TxRef* and RxRef* signals are not synchronized to either TxClk or RxClk. Thus, this is not further described here.
2. Operation and Timing, which is fully described, and changed in the following manner :
    1. Cell and Octet-Level Handshakes - Minimal text changes for clarification
    2. Examples - Fully rewritten
    3. Timing - Eliminated from these chapters. Chapter 5 of this document provides details on timing at various speeds including 25 MHz.

3.2. Level 1 Section 4.2 on Transmit Operation

The Transmit interface is controlled by the ATM layer. The ATM layer provides an interface clock to the PHY layer for synchronizing all interface transfers. This convention requires the PHY layer to incorporate rate-matching buffers (i.e. a FIFO).

The transmit interface has data flowing in the same direction as the ATM enable. The ATM transmit block generates all output signals on the rising edge of the TxClk. Signals TxData, TxSOC, and TxPrty are sampled on the rising edge of TxClk. Signals TxEnb* and TxFull*/TxClav do not necessarily have to be sampled.

Transmit data is transferred from the ATM layer to PHY layer via the following procedure. The PHY layer indicates it can accept data using the TxFull*/TxClav signal, then the ATM layer drives data onto TxData and asserts TxEnb*. The PHY layer controls the flow of data via the TxFull*/TxClav signal.

3.2.1. Octet-Level Handshake

During a time period termed the *transmit window*, the PHY layer stores data from TxData on the low-to-high transition of TxClk, if TxEnb* is asserted. The transmit window exists from the time that the PHY layer indicates it can accept data by deasserting TxFull*, until 4 valid write cycles after the PHY layer asserts TxFull*. The PHY layer may assert TxFull* at any time. After being asserted this indicates that the ATM layer may transfer no more than 4 data words on TxData until TxFull* is deasserted again.

The ATM layer must deassert TxEnb* within 4 data writes of TxFull* assertion and must not reassert TxEnb* until TxFull* is detected deasserted.[2] Asserting TxEnb* outside the transmit window is an error, and the PHY layer will ignore such writes. Inside the transmit window the ATM layer may assert and deassert TxEnb* as required.

[2]This rule allows the ATM layer to exactly determine during which cycles data was transferred on TxData.

3.2.2. Cell-Level Handshake

The cell-level handshake is identical to the octet-level handshake except for one difference, namely that once TxClav is asserted, the PHY layer must be capable of accepting the transfer of a whole cell. TxEnb* can be used by the ATM Layer to control the flow of data at an octet level (just as for octet-level handshake mode). To ensure that the ATM Layer does not cause transmit overrun, the PHY Layer must deassert TxClav at least 4 cycles before the end of a cell if it cannot accept the immediate transfer of the subsequent cell. As a suggestion, if a PHY device using cell level handshake is being connected to a byte based ATM device, the TxClav signal should remain asserted until 4 cycles before the end of a cell.

3.2.3. Examples

The timing sequences may be summarized as: TxEnb* asserted indicates valid ATM data available in the current cycle, TxFull* asserted indicates the PHY is unable to accept new data after 4 more write cycles, TxClav deasserted indicates the PHY is unable to accept another cell transfer after the current one.

Figure 3.1 and 3.2 show the octet-level handshaking between the PHY and ATM layer. In figure 3.1 and on clock edge 2, the ATM layer recognizes that TxFull* was asserted by the PHY and, as a consequence of this, it deasserts TxEnb* after maximum 4 more write cycles, i.e. on clock edge 6. On clock edge 9, the ATM layer detects TxFull* deasserted and continues transmitting valid data by asserting TxEnb* and driving P47 on TxData. This is the minimum reaction time of TxEnb* reacting to TxFull*. A slower ATM layer could need more clock cycles to assert TxEnb*. On clock edge 12, the ATM layer has no valid data to transmit and interrupts the data transmission by deasserting TxEnb*. The ATM layer continues transmitting data by driving TxEnb* to low again on clock edge 13. TxEnb* deasserted is always indicating invalid data on TxData which is shown in the diagram by using X's.

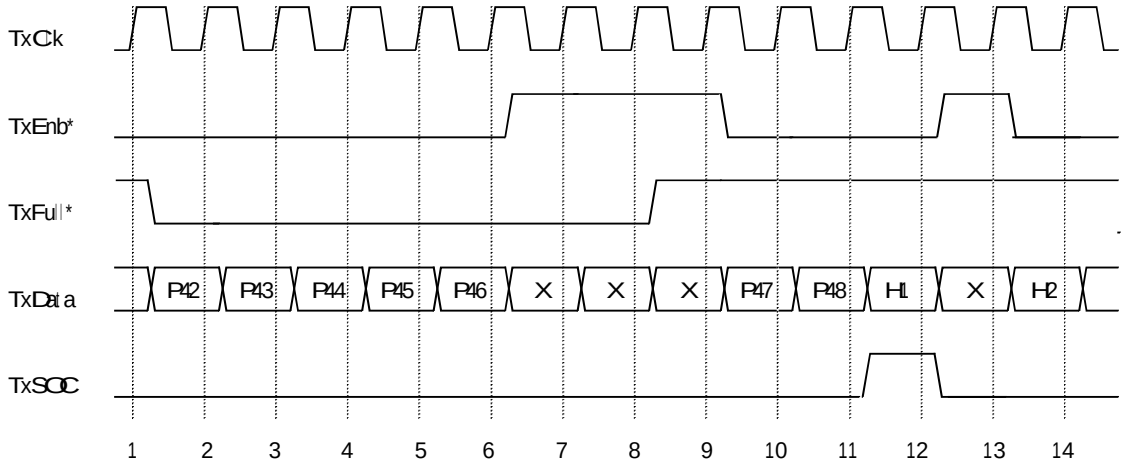


Figure 3.1. Transmit timing for octet-level handshake (example 1)

Figure 3.2 shows the case where TxEnb* does not react to TxFull* asserted because TxFull* is deasserted again before TxEnb* was deasserted. On clock edge 3, the ATM layer detects TxFull* deasserted and starts the transmission of valid data. On clock edge 6, the ATM layer detects TxFull* asserted and prepares TxEnb* to be deasserted on clock edge 10. Before the transmission interruption can take place, the ATM layer detects TxFull* deasserted again on

clock edge 9 and, as a consequence, keeps TxEnb* asserted. A real implementation may probably not act like this and will deassert TxEnb* for a few clock cycles but from a strict signal definition point of view this may very well happen.

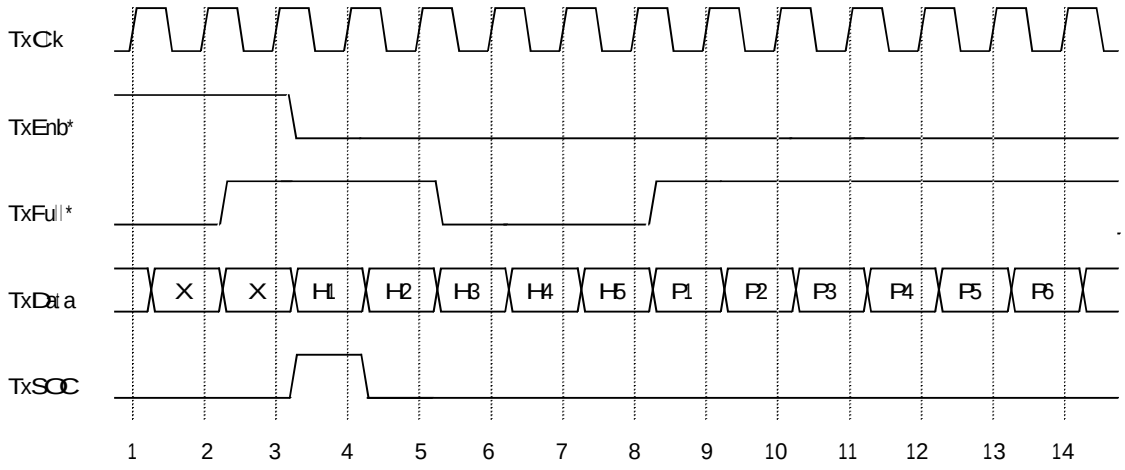


Figure 3.2. Transmit timing for octet-level handshake (example 2)

Figure 3.3 to 3.6 show the cell-level handshaking between the PHY and ATM layer. In figure 3.3 and on clock edge 2, the ATM layer recognizes that TxClav was asserted by the PHY and starts to transmit a complete cell. The PHY indicates 4 cycles before the end of the cell (i.e. on clock edge 51) whether it can accept an additional cell. In this example, the PHY cannot accept an additional cell and, as a consequence, the ATM layer deasserts TxEnb* on clock edge 55. Once TxClav indicates that the PHY can accept a cell, it should stay asserted until the PHY recognizes that the ATM layer has transmitted payload byte 43 of that cell. The PHY must indicate that it cannot accept another cell at least 4 write cycles before the end of the cell. It is recommended that the PHY layer keep this signal asserted until 4 cycles before the end of the cell.

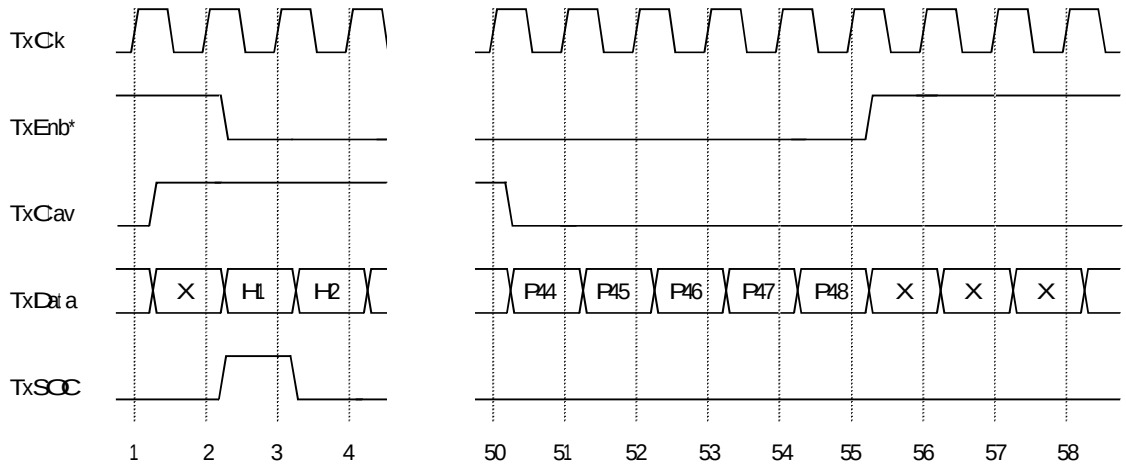


Figure 3.3. Transmit timing for cell-level handshake (example 1)

Figure 3.4 shows an example where the PHY indicates on clock edge 3 that it can accept another cell from the ATM layer. Therefore, the ATM layer starts transmitting the next cell immediately

after P48. Like with the octet-level-handshake, the ATM layer can interrupt data transmission at any time by deasserting TxEnb* which is shown here between clock edge 11 and 12.

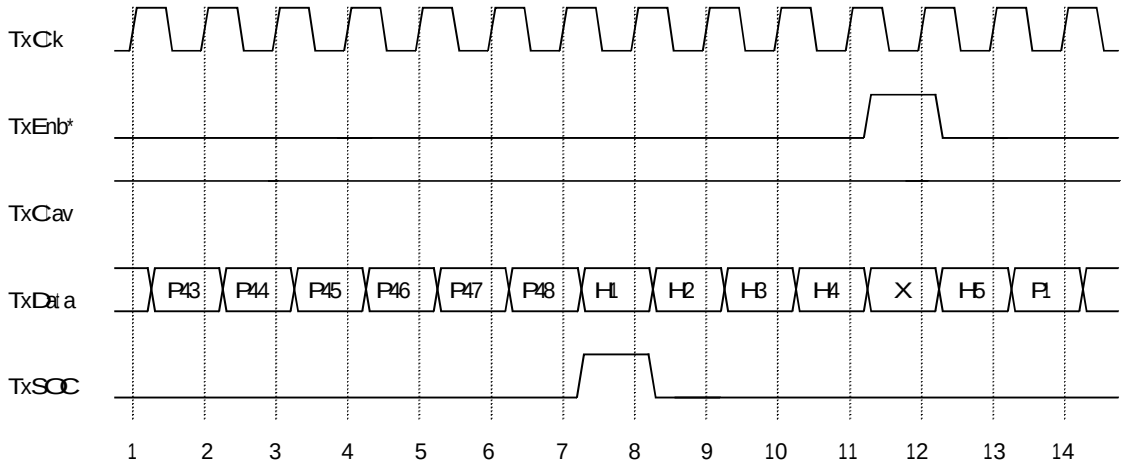


Figure 3.4. Transmit timing for cell-level handshake (example 2)

Figure 3.5 shows an example where the PHY indicates on clock edge 3 that it cannot accept another cell from the ATM layer. Before the ATM layer can interrupt data transmission by deasserting TxEnb* on clock edge 7, it detects on clock edge 5 that the PHY can again accept another cell. Therefore, the ATM layer keeps TxEnb* asserted and transmits the next cell immediately after P48.

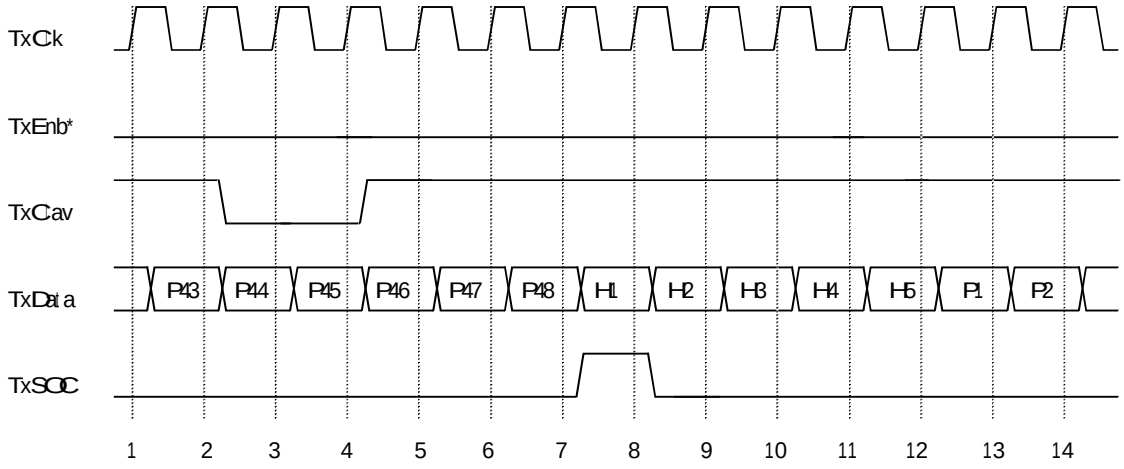


Figure 3.5. Transmit timing for cell-level handshake (example 3)

Figure 3.6 shows an example where the PHY indicates on clock edge 3 that it cannot accept another cell from the ATM layer. Independent of that indication, the ATM layer interrupts data transmission on clock edge 4 by deasserting TxEnb* because it has no data to send. However, it knows that P45 was not the last octet of the cell and that the PHY can still accept 3 more octets. Therefore, it asserts TxEnb* on clock edge 6 (P46 is now available in the ATM layer) and continues data transmission until the last cell octet. As TxClav is still not asserted on clock edge

9, the ATM layer stops data transmission by deasserting TxEnb* again. On clock edge 12, the ATM layer detects TxClav asserted and starts the next cell transfer.

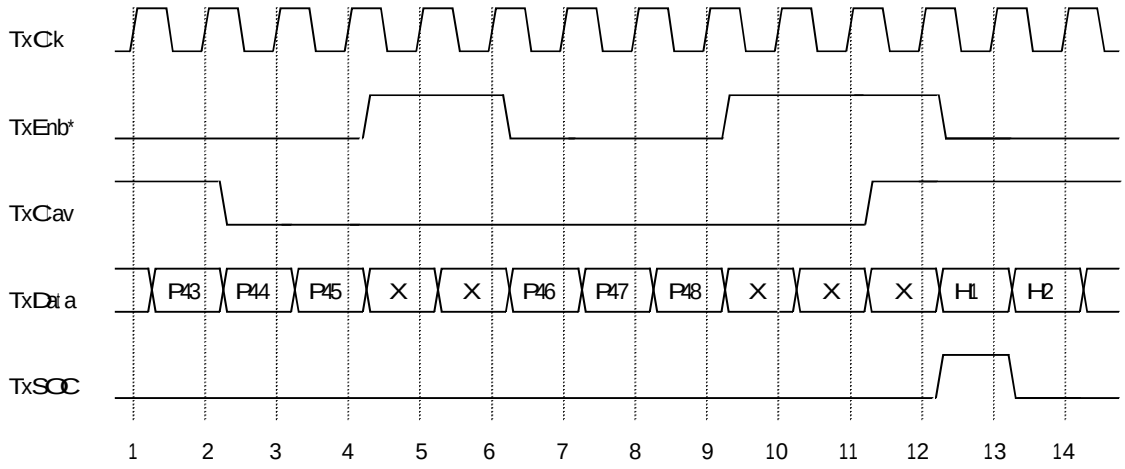


Figure 3.6. Transmit timing for cell-level handshake (example 4)

Some of these examples might never take place in a certain implementation but, according to the signal definition, they are in principle possible and should be taken into account when designing the corresponding devices.

3.3. Level 1 Section 5.2 on Receive Operation

The Receive interface is controlled by the ATM layer. The ATM layer provides an interface clock to the PHY layer to synchronize all transfers. This convention requires the PHY layer to incorporate rate-matching buffers (i.e. a FIFO).

The receive interface has data flowing in the opposite direction to the ATM layer enable. The transmit interface has data flowing in the same direction as the ATM enable. The ATM receive block generates all output signals on the rising edge of the RxClk. Signals RxData, RxSOC, and RxPrty are sampled on the rising edge of RxClk. Signals RxEnb* and RxEmpty*/RxClav do not necessarily have to be sampled.

Receive data is transferred from the PHY layer to ATM layer via the following procedure. The PHY layer indicates it has valid data, then the ATM layer asserts RxEnb* to read this data from the PHY layer. The PHY layer indicates valid data (thereby controlling the data flow) via the RxEmpty*/RxClav signal.

3.3.1. Octet-Level Handshake

The PHY layer indicates it has valid data in any cycle by deasserting RxEmpty*. The PHY layer may assert and deassert RxEmpty* at any time[3]. The ATM layer indicates that it wants to read PHY data by asserting RxEnb*. The ATM layer may assert and deassert RxEnb* at any time.[4]

[3]An implementation could deassert RxEmpty* after several bytes are available (e.g. a cell header has been received and checked).
[4]This means that the ATM layer can choose to permanently assert RxEnb* if desired.

The cycles during which RxEnb* is asserted constitute a *read window*. During a read window the PHY layer reads data from its internal FIFO and presents it on RxData/RxSOC on each low-to-high transition of RxClk. Asserting RxEnb* while RxEmpty* is asserted is not an error but the value of RxData is undefined.

3.3.2. Cell-Level Handshake

The cell-level handshake is identical to the octet-level handshake except for one difference, namely that once RxClav is asserted, the PHY layer must be able to transfer a whole cell. RxClav has the same timing as RxEmpty*. This means that in the cycle following the one with the final octet of the cell, RxClav asserted indicates there is a new cell to transfer, while RxClav deasserted indicates there is no new cell to transfer.

3.3.3. Examples

The timing sequences may be summarized as: RxEnb* forces a data read from the PHY layer when RxClav is asserted, the PHY layer drives data during a cycle after one at which RxEnb* was asserted and RxClav was asserted.

Figure 3.7 shows the octet-level handshaking between the PHY and ATM layer. In figure 3.7 and on clock edge 2, the ATM layer recognizes that RxEmpty* was deasserted by the PHY and, as a consequence of this, it asserts RxEnb*. The PHY detects RxEnb* asserted on clock edge 3 and drives the first cell octet on RxData. Between clock edge 5 and 6, the PHY runs out of data and indicates invalid data on RxData by asserting RxEmpty*. On clock edge 10, the ATM cannot accept additional data and therefore it drives RxEnb* deasserted in the previous cycle. The ATM layer continues the transfer on clock edge 12 by asserting RxEnb* on clock edge 11. RxData and RxSOC are tri-stated when RxEnb* has been deasserted in the previous cycle. The meaning of RxEmpty* depends on RxEnb*: between clock edge 1 and 3 (RxEnb* has been deasserted in the previous cycle), RxEmpty* indicates the availability of an octet to transfer. The same is true for the time interval between clock edge 10 and 12. Between clock edge 3 and 10 (RxEnb* has been asserted in the previous cycle), RxEmpty* indicates valid/invalid data on RxData. The same is true for the time after clock edge 12.

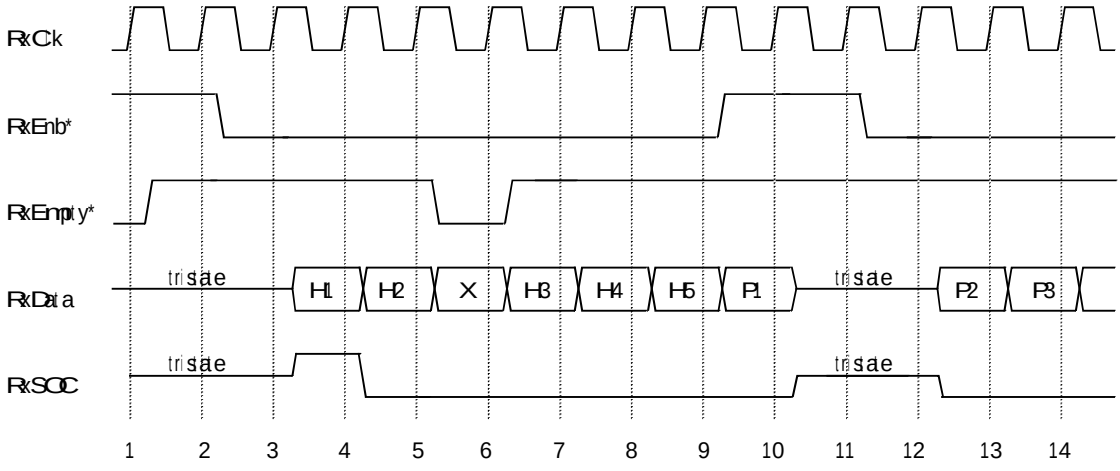


Figure 3.7. Receive timing for octet-level handshake

Figure 3.8 to 3.10 give examples for cell-level handshaking between the PHY and ATM layer. In figure 3.8 and on clock edge 2, the ATM layer deasserts RxEnb* while P48 is on RxData because the ATM layer knows (e.g. by means of a counter) that P48 is the last octet of the cell. As a consequence, the PHY indicates cell availability on clock edge 3 and drives in this example RxClav to low indicating that no new cell is available. On clock edge 5, the PHY indicates the availability of a new cell and, as a consequence, the ATM layer asserts RxEnb* on clock edge 6 and the PHY starts the cell transfer on clock edge 7. Expecting the final octet of the cell (on clock edge 60), the ATM layer indicates RxEnb* deasserted in order to force RxClav to indicate the availability of a new cell. On clock edge 61, the ATM detects RxClav asserted and drives RxEnb* low again to start the transfer of the new cell. Again, the meaning of RxClav depends on RxEnb*: between clock edge 1 and 3 (RxEnb* has been asserted in the previous cycle), RxClav indicates valid data on RxData. The same is true for the time interval between clock edge 7 and 60 and after clock edge 62. Between clock edge 3 and 7 (RxEnb* has been deasserted in the previous cycle), RxClav indicates the availability of a new cell. The same is true for the time interval between clock edge 60 and 62. Note, that 2 extra clock cycles (clock edge 60 to 62) are the minimum time that is needed to check availability of a new cell when the ATM layer deasserts RxEnb* at P48.

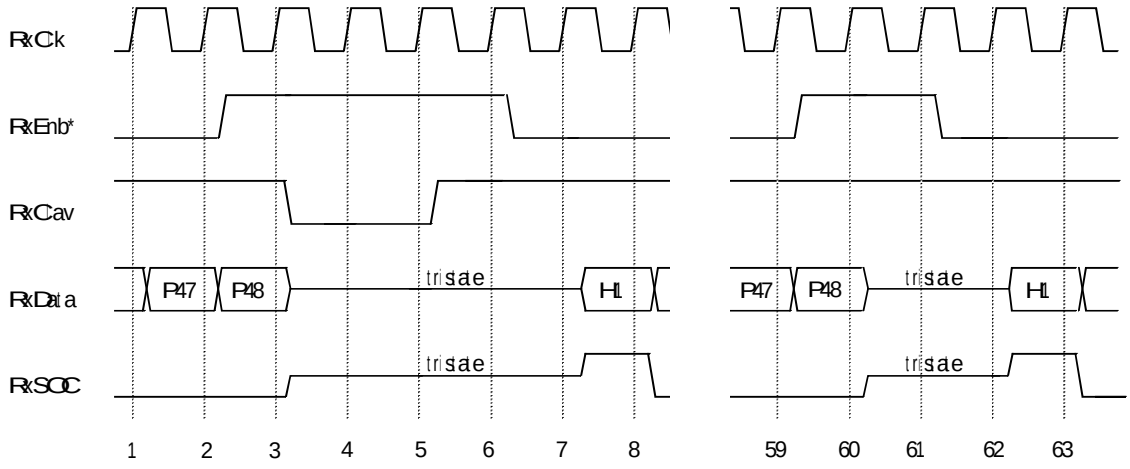


Figure 3.8. Receive timing for cell-level handshake (example 1)

Figure 3.9 shows an example where cell transfer completion is indicated by driving RxClav low showing invalid data on RxData. On clock edge 4, RxClav indicates invalid data on RxData. The cell transfer must have been completed because the PHY does not output invalid data during cell transfer. The ATM layer does not react on the indication, but simply keeps RxEnb* asserted. On clock edge 5 the PHY has a new cell to transfer and starts immediately data transmission by indicating valid data on RxData. On clock edge 59, the ATM layer detects by observing RxClav deasserted that cell transfer has been completed and deasserts RxEnb*. As a consequence, the PHY tri-states RxData/RxSOC on clock edge 60 and RxClav indicates that no new cell is available.

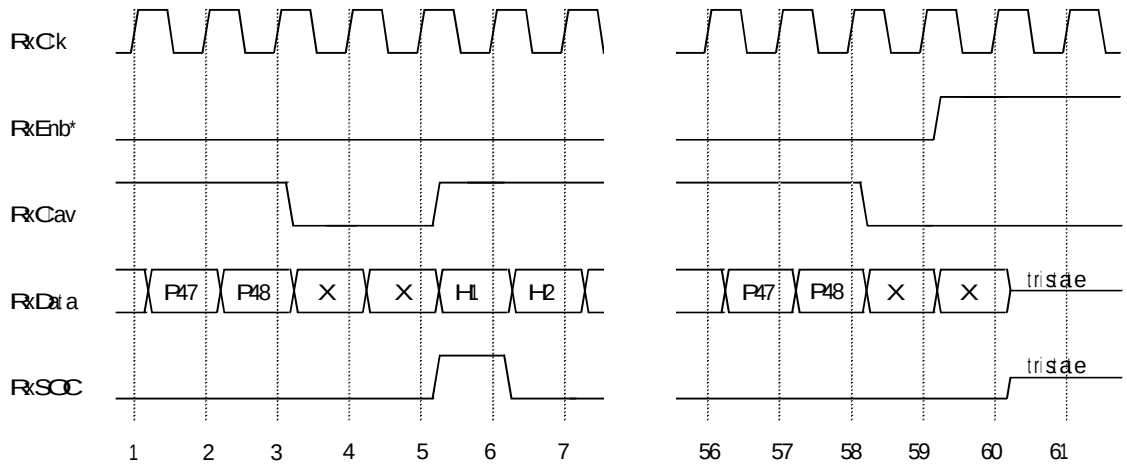


Figure 3.9. Receive timing for cell-level handshake (example 2)

Figure 3.10 shows an example where the ATM layer interrupts the cell transfer by deasserting RxEnb* on clock edge 43 and continues the cell transfer by asserting RxEnb* on clock edge 47. Note that RxClav stays asserted between clock edge 44 and clock edge 48 indicating the availability of the cell currently transmitted.

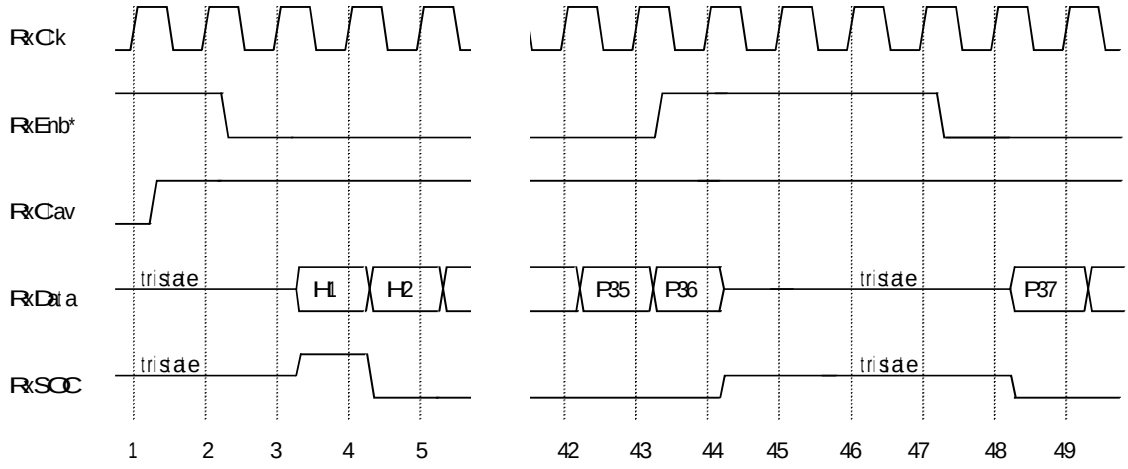


Figure 3.10. Receive timing for cell-level handshake (example 3)

4. MPHY Data Path Operation

This section describes several methods for MPHY operation summarized as : Operation with 1 TxClav and 1 RxClav, Direct Status Indication, and Multiplexed Status Polling.

The following MPHY method is defined as required (**R**) for Utopia Level 2 MPHY operation.

1. Operation with 1 TxClav and 1 RxClav, described in section 4.2.

The following MPHY schemes are defined as optional (**O**) for Utopia Level 2 MPHY operation.

1. Direct Status Indication, described in section 4.3.
2. Multiplexed Status Polling, described in section 4.4.

4.1. Signals

4.1.1. Transmit Interface

This section defines new signals for the Transmit interface in relation to the Level 1 specification, along with a minor enhancement to one of the existing signals, retaining forward and backward compatibility.

The following existing signals are modified for the Multi-PHY Transmit interface :

TxFull*/TxClav [0]
: Cell Available. For cell-level flow control in an MPHY environment, TxClav is an active high tri-stateable signal from the MPHY to ATM layer. A polled MPHY device (port) drives TxClav only during each cycle following one with its address on the TxAddr lines. The polled MPHY device (port) asserts TxClav high to indicate it can accept the transfer of a complete cell, otherwise it deasserts the signal. Note the change in the label for the signal to TxClav [0].

The following additional signals are defined as required (**R**) for the Multi-PHY Transmit interface.

TxAddr[4..0]
: Address. Five bit wide true data driven from the ATM to MPHY layer to poll and select the appropriate MPHY device (port in presence of multiple TxClav signals). TxAddr[4] is the MSB. Each MPHY device needs to maintain its address. This value should be programmed through the management interface. The value for the Tx and Rx portions of an MPHY device (port in presence of multiple TxClav signals) should be identical. Address 31 indicates a null PHY port.

The following additional signals are defined as optional (**O**) for the Multi-PHY Transmit interface.

TxClav[3..1]
: Additional Cell Available Signals. A PHY device (as opposed to a PHY port) may include a total of up to 4 TxClav signals corresponding to 4 PHY ports, which may be used either for direct status indication or for multiplexed status polling (see chapter 4.3, 4.4). The operation of each is identical to that of TxClav[0].

The following additional signals are defined as required (**R**) for operation in 16-bit mode.

TxData[15:8]
: High octet of data. Most significant octet of transmit data, driven from ATM to PHY. TxData[15] is the MSB, TxData[0] is the LSB of the 16-bit data path.

The following existing optional (O) signals are modified for operation in 16-bit mode.

TxPrty
: Data path Parity. The TxPrty parity bit is modified in 16-bit mode to serve as the odd parity bit over TxData [15:0].

4.1.2. Receive Interface

This section defines new signals for the Receive interface in relation to the Level 1 specification, along with a minor enhancements to some of the existing signals, retaining forward and backward compatibility.

The following existing signals are modified as described below :

RxData[7..0]
: Data. To support multiple PHY configurations, RxData must be tri-stateable, enabled only in cycles following those with RxEnb* asserted.

RxSOC
: Start Of Cell. To support multiple PHY configurations, RxSOC must be tri-stateable, enabled only in cycles following those with RxEnb* asserted.

RxEnb*
: Enable. In multiple PHY configurations, RxEnb* is used to tri-state RxData and RxSOC PHY layer outputs.

RxEmpty*/RxClav [0]
: Cell Available. For cell-level flow control in an MPHY environment, RxClav is an active high tri-stateable signal from the MPHY to ATM layer. A polled MPHY device (port) drives RxClav only during each cycle following one with its address on the TxAddr lines. The polled MPHY device asserts RxClav high to indicate it has a complete cell available for transfer to the ATM layer, otherwise it deasserts the signal.

The following additional signals are defined as required (**R**) for the MPHY Receive interface :

RxAddr[4..0]
: Address. Five bit wide true data driven from the ATM to MPHY layer to select the appropriate MPHY device (port in presence of multiple RxClav signals). RxAddr[4] is the MSB. Each MPHY device needs to maintain its address. This value should be programmed through the management interface. The value for the Tx and Rx portions of an MPHY device (port in presence of multiple RxClav signals) should be identical. Address 31 indicates a null PHY port.

The following additional signals are defined as optional (**O**) for the Multi-PHY Receive interface.

RxClav[3..1]
: Additional Cell Available Signals. A PHY device (as opposed to a PHY port) may include a total of up to 4 RxClav signals corresponding to 4 PHY ports, which may be used either for direct status indication or for multiplexed address polling. The operation of each is identical to that of RxClav [0].

The following additional signals are defined as required (**R**) for operation in the 16-bit mode :

RxData[15:8]
: High octet of data. Most significant octet of receive data, driven from PHY to ATM. RxData[15] is the MSB, RxData[0]is the LSB of the 16-bit data path.

The following existing optional (O) signals are modified for operation in 16-bit mode.

RxPrty
: Data path Parity. The RxPrty parity bit is modified in 16-bit mode to serve as the odd parity bit over RxData [15:0]. To support multiple PHY configurations, RxData must be tri-stateable, enabled only in cycles following those with RxEnb* asserted.

4.2. Operation with 1 TxClav & 1 RxClav Signal

4.2.1. Transmit Interface

4.2.1.1. MPHY Layer Cell-Level Handshake with 1 TxClav

In Level 1 Utopia there is only one PHY layer device, and it utilizes TxClav to convey transfer status to the ATM layer. In Level 2 Utopia, only one MPHY port at a time is selected for a cell transfer. However, another MPHY port may be polled for its TxClav status while the selected MPHY port (device) transfers data.

The ATM layer polls the TxClav status of a MPHY port by placing its address on TxAddr. The MPHY port (device) drives TxClav during each cycle following one with its address on the TxAddr lines.

The ATM layer selects a MPHY port for transfer by placing the desired MPHY port address onto TxAddr, when TxEnb* is deasserted during the current clock cycle, and asserted during the next clock cycle. All MPHY devices only examine the value on TxAddr for selection purposes when TxEnb* is deasserted. The MPHY port is selected starting from the cycle after its address is on the TxAddr lines, and TxEnb* is deasserted; and ending in the cycle a new MPHY port is addressed for selection, and TxEnb* is deasserted.

Once a MPHY port is selected the cell transfer is accomplished as described by the cell-level handshake of Utopia Level 1.

To operate an MPHY device in a single PHY environment, the address pins should be set to the value programmed by the management interface.

4.2.1.2. Examples with 1 TxClav

Figure 4.1 shows an example where PHYs are polled until the end of a cell transmission cycle. The TxClav signal shows that PHYs N-3 and N+3 can accept cells and PHY N+3 is selected.

With the rising clock edge #16 in Figure 4.1 the PHY is selected. Immediately after the beginning of cell transmission to PHY N+3 the ATM layer starts polling again. Using the 2-clock polling cycles shown in Figure 4.1 up to 26 PHYs can be polled. This maximum value can only be reached if all responses occur in minimum delays, e.g. as shown in Figure 4.1, where with clock edge #15 the response of the last PHY is obtained, immediately followed by the TxEnb* pulse to the PHYs. If an ATM implementation needs additional clock cycles to select the PHY less than 26 PHY can be polled during one cell cycle. Note that if the ATM would decide to select PHY N again for the next cell transmission it could leave the TxEnb* line asserted and start transmitting the next cell with clock edge #15. This would result in a back-to-back cell transmission.

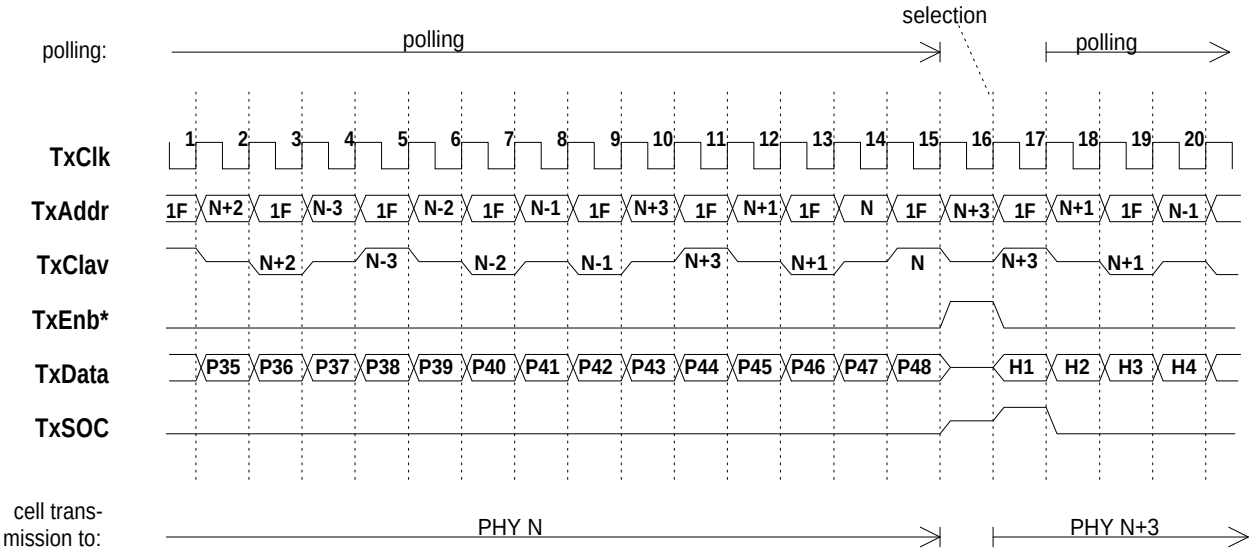


Figure 4.1. Polling phase and selection phase at transmit interface

Note that the active PHY (PHY N) itself is polled in octet P48. According to the UTOPIA level 1 specification at this time the TxClav signal of the PHY yet indicates the possibility of a subsequent cell transfer. Polling of PHY N before octet P44 would be possible, but does not indicate availability of the next cell.

In Figure 4.2 an example is given where the transmission of cells via the transmit interface is stopped by the ATM as no PHY is ready to accept cells. Polling continues. Some clock cycles later one PHY gets ready to accept a cell. During the transmission pause the TxData and TxSOC may go into high impedance state as shown in Figure 4.2. TxEnb* is held in deasserted state. When a PHY is found which is ready to accept a cell - in case of Figure 4.2 it is PHY N+3 - the address of this PHY must be applied again to select it. This is necessary due to the 2-clock polling cycle, where the PHY is detected at the clock edge #15 in Figure 4.2. At this time the address of PHY N+3 is not on the bus any more. It must be applied again in the next clock cycle. With clock edge #16 PHY N+3 is selected.

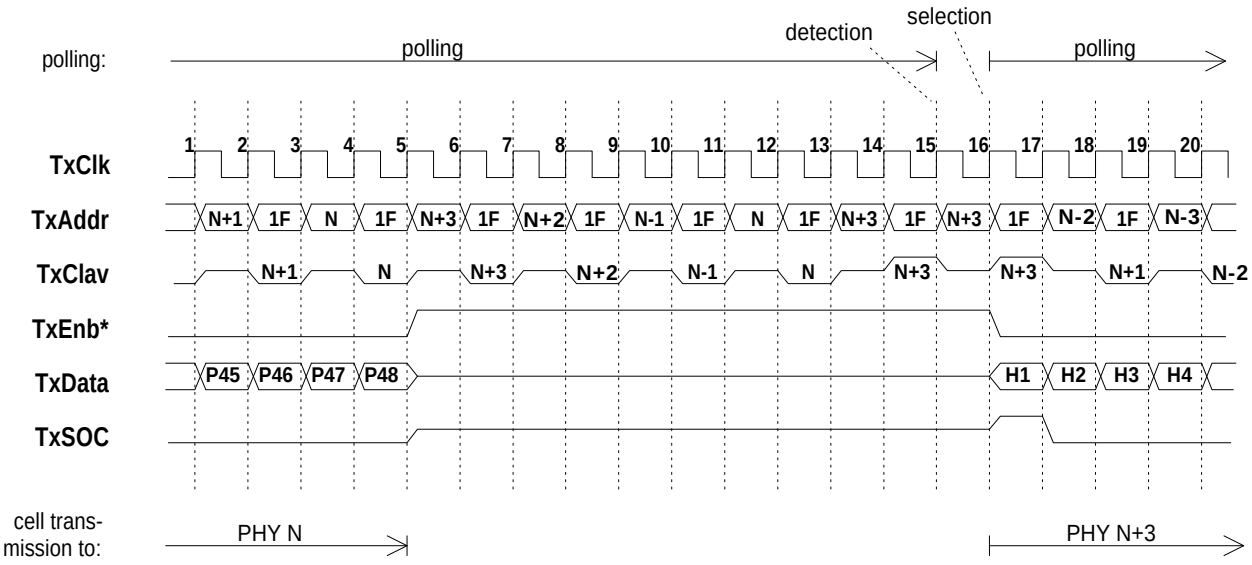


Figure 4.2. End and restart of cell transmission at transmit interface

Figure 4.3 shows an example where the ATM must pause the data transmission, as it has no data available - in this case for three clock cycles. This is done by deasserting TxEnb* and (optionally) setting TxData and TxSOC into high impedance state. Polling may continue. In the last clock cycle before restarting the transmission the address "M" of the previously selected PHY shall be put on the TxAddr bus to re-select PHY M again.

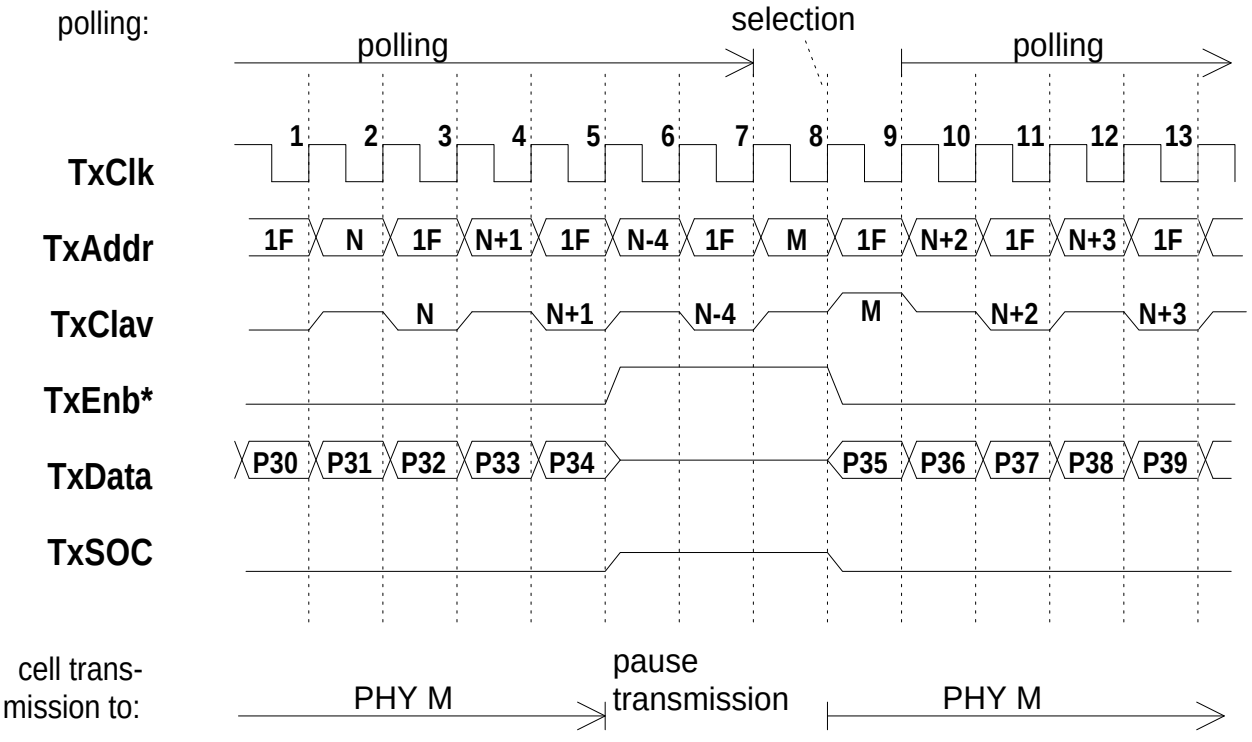


Figure 4.3. Transmission to PHY paused for three cycles

Note that the example shown in Figure 4.3 is theoretically possible, but is only an option for the ATM layer.

4.2.2. Receive Interface

4.2.2.1. MPHY Cell-Level Handshake with 1 RxClav

In Level 1 Utopia there is only one PHY layer device, and it utilizes RxClav to convey transfer status to the ATM layer. In Level 2 Utopia, only one MPHY port at a time is selected for a cell transfer. However, another MPHY port may be polled for its RxClav status while the selected MPHY port transfers data.

The ATM layer polls the RxClav status of a MPHY port by placing its address on RxAddr. The MPHY port (device) drives RxClav during each cycle following one with its address on the TxAddr lines.

The ATM layer selects a MPHY port for transfer by placing the desired MPHY port address onto RxAddr, when RxEnb* is deasserted during the current clock cycle and asserted during the next clock cycle. All MPHY devices only examine the value on RxAddr for selection purposes when RxEnb* is deasserted. The MPHY port is selected starting from the cycle after its address is on the RxAddr lines, and RxEnb* is deasserted; and ending in the cycle a new MPHY port is addressed for selection, and RxEnb* is deasserted.

Once a MPHY port is selected the cell transfer is accomplished as described by the cell-level handshake of Utopia Level 1.

To operate an MPHY device in a single PHY environment, the address pins should be set to the value programmed by the management interface.

4.2.2.2. Example with 1 RxClav

Figure 4.4 shows the corresponding case to Figure 4.1 for the receive interface. During reception of a cell from PHY N the other PHYs are polled. It turns out that PHY N-3 and PHY N+3 have cells available, and finally PHY N+3 is selected. (Remember that the PHY number values are for example only.) As at the transmit interface the 2-clock polling cycles allow up to 26 PHYs to be polled in the 8-bit mode, and up to 13 PHYs in the 16-bit mode.

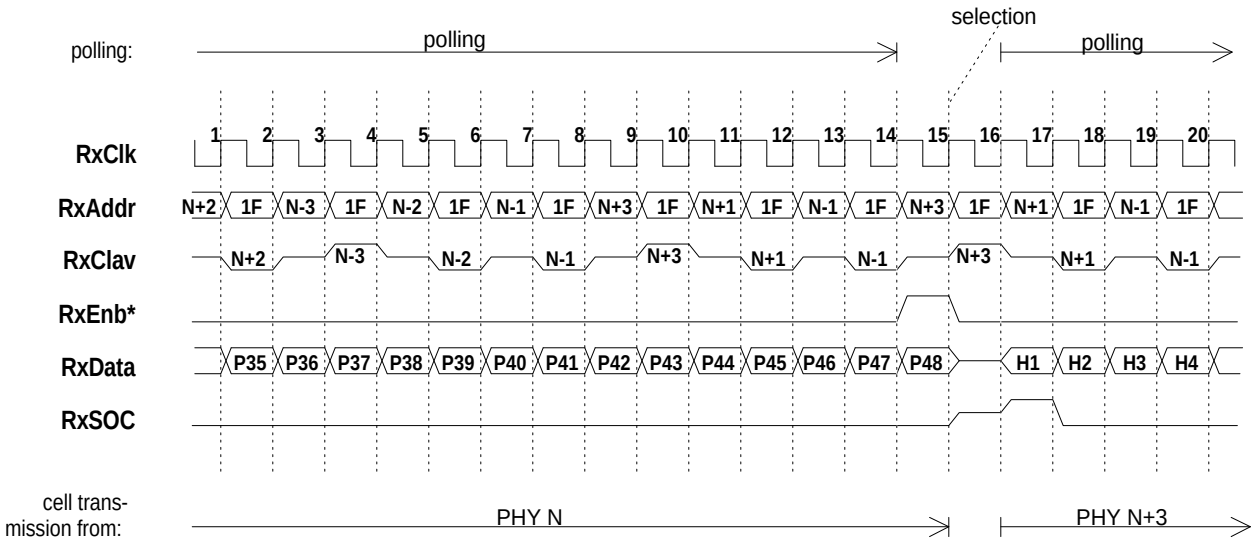


Figure 4.4. Polling phase and selection phase at receive interface

Figure 4.5 shows the corresponding case to Figure 4.2 for the receive interface. After the end of transmission of a cell from PHY N no other PHY has a cell available. Therefore RxEnb* remains asserted, as the ATM assumes a cell available from PHY N. With clock edge #9 it turns out that also PHY N has no cell available, as RxSOC remains low. The ATM then deasserts RxEnb* while the polling of the PHYs continues. With clock edge #15 PHY N-3 is found to have a cell for transmission. So address N-3 is applied and the PHY N-3 is selected with clock edge #16.

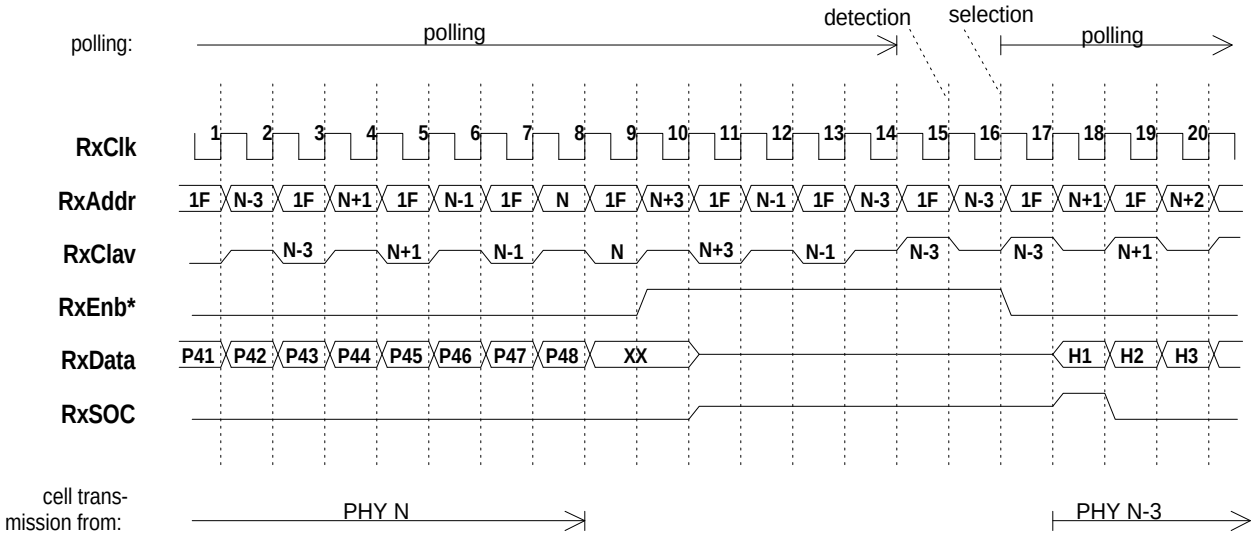


Figure 4.5. End and restart of cell transmission at receive interface

Figure 4.6 shows a case where, PHY N has a cell available, one cycle after the end of transmission of its current cell. Since RxEnb* was still active in previous cycle, PHY N is required to activate the RxSOC signal and place a valid H1 byte during clock cycle 10 on the RxData bus. The ATM device is required to receive this byte even though the RxClav signal was deasserted during the previous cycle. The ATM device utilizes the RxSOC signal to realize that the PHY placed valid data on the RxData bus. It must reselect PHY N even if another PHY

device indicates that it has an available cell to prevent data from different cells from mixing internally.

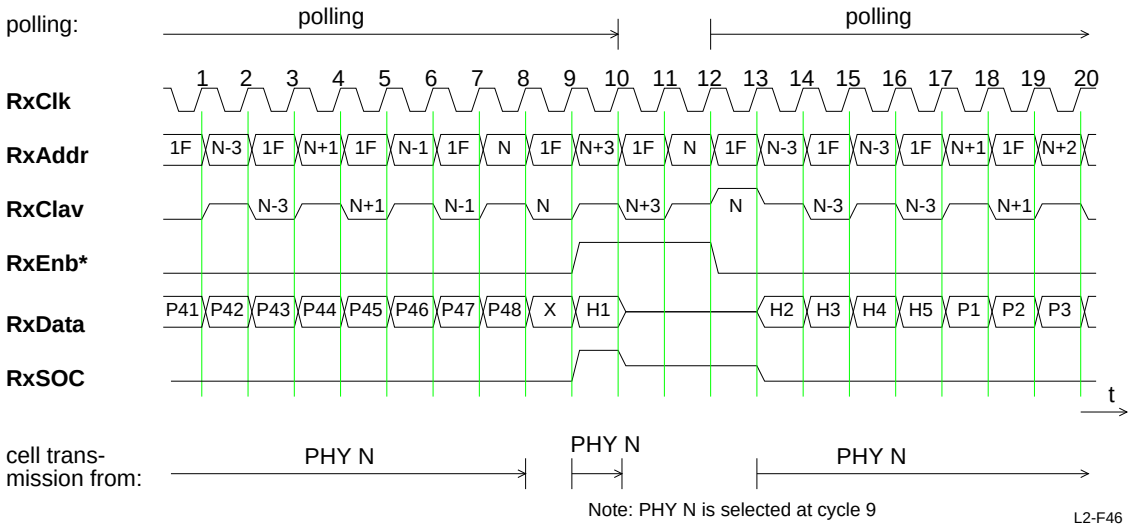


Figure 4.6. Unexpected receipt of two back to back cells from the same PHY

Figure 4.7 shows a case where two subsequent cells are transmitted from the same PHY, PHY N. As no other PHY signals an available cell via the RxClav line at the end of cell transmission, the ATM assumes a further cell from PHY N and lets the RxEnb* line asserted. In this case there is indeed a subsequent cell from PHY N available, which the ATM recognizes with the RxSOC signal going high with clock edge #8. The result is a back-to-back cell transmission.

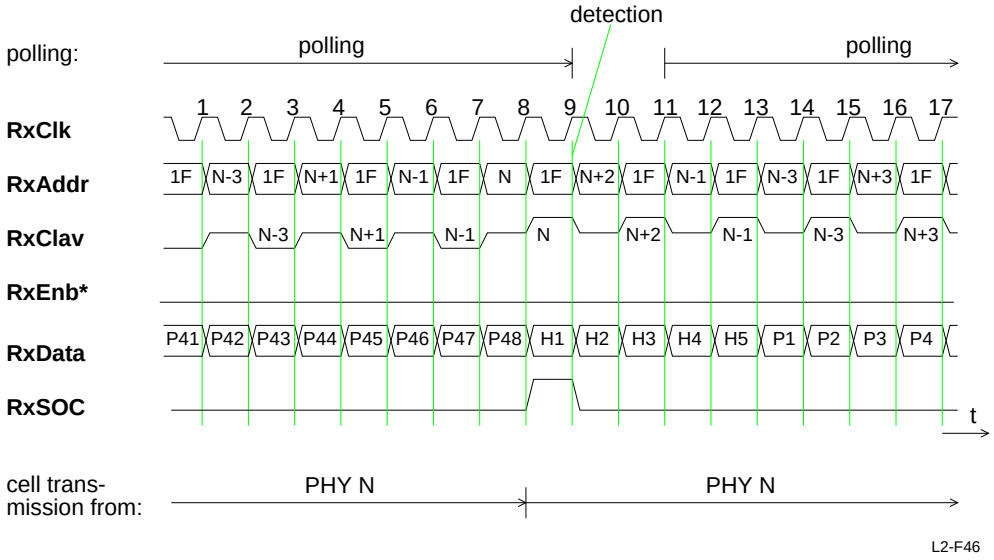


Figure 4.7. Two subsequent cells from same PHY

Figure 4.8 finally shows the corresponding case to Figure 4.3 for the receive interface. The cell transmission from PHY M is halted for three octet cycles by the ATM. Polling continues. Before RxEnb* is asserted again the address of the actually selected PHY has to be output by the ATM

to re-select the same PHY (with clock edge #9). As at the transmit interface this feature is optional for the ATM layer but mandatory for the PHY.

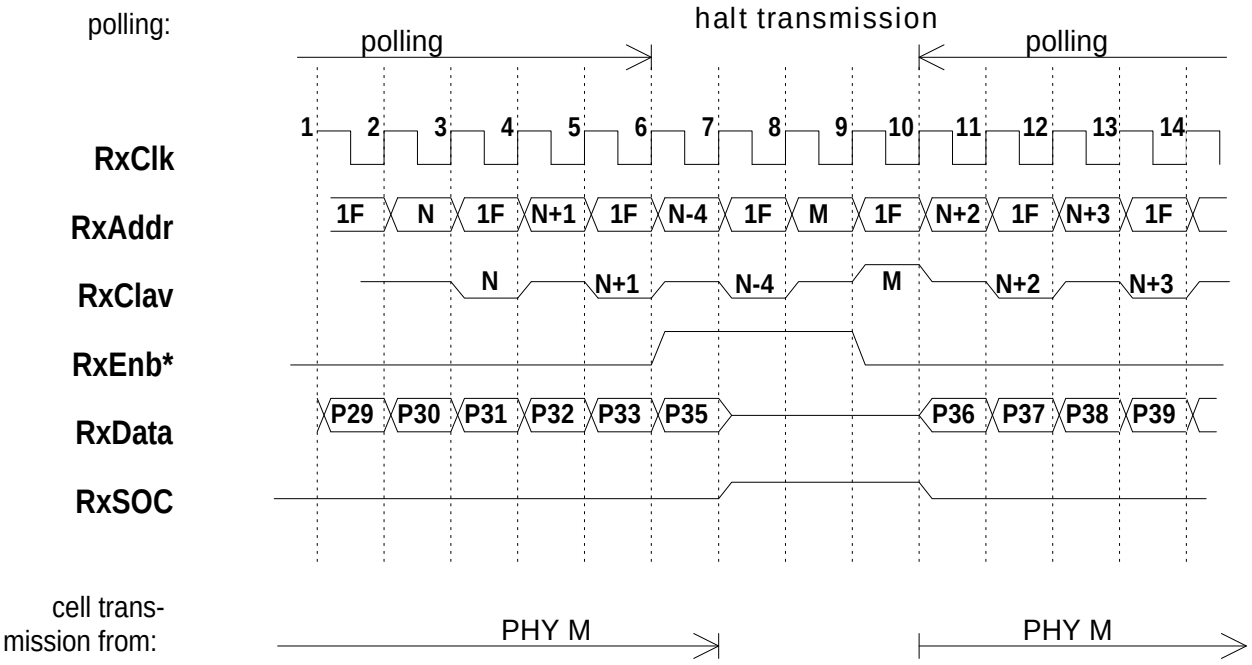


Figure 4.8. Transmitting PHY halted temporarily by the ATM Layer

4.3 Direct status indication

4.3.1 Method

Let us consider up to max. four PHY ports connected to one ATM layer, see Figure 4.9. For each PHY port, the status signals RxClav and TxClav are permanently available according to UTOPIA Level 1 specification. PHY devices with up to four PHY ports on-chip have up to four RxClav and up to four TxClav status signals, one pair of RxClav and TxClav for each PHY port. In case of less then four PHY ports per device, nevertheless these PHY devices may have up to four status signal pairs. Note, in principle any unique port address can be assigned to the four PHY ports. In Figure 4.9 the addresses #1 to #4 are just an example.

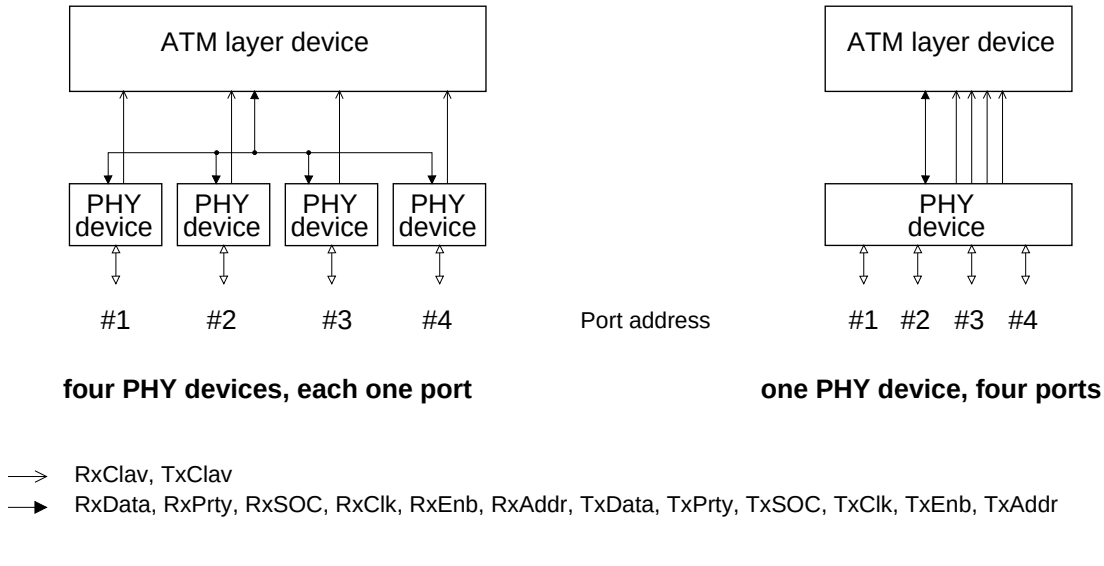


Figure 4.9. Maximal four PHY ports connected to one ATM layer device

Status signals and cell transfers are independent of each other. No address information is needed to obtain status information. Address information must be valid only for selecting a PHY port prior to one or multiple cell transfers.

With respect to the status signals RxClav and TxClav, this mode of operation corresponds to that of four individual PHY devices according to Utopia level 1. With respect to the cell transfer, this mode of operation corresponds to that as described in other parts of this document. The ATM layer selects a PHY port for cell transfer by placing the desired port on the address lines (RxAddr[4:0], TxAddr[4:0]), while the enable signal (RxEnb*, TxEnb*) is deasserted. All PHY ports only examine the value on the address lines for possible selection when the enable signal is deasserted.

In case the ATM suspends transmission for a specific PHY port during a cell transfer, no cells to/from other PHY ports can be transferred during this time.

4.3.2 Examples

4.3.2.1 Receive direction

Examples for the receive direction are given in Figure 4.10 and 4.11. The status signals RxClav[3:0] are associated to PHY port addresses #4, #3, #2 and #1, see Figure 4.3. Note, in principle any port address can be assigned to the four PHY ports. There is no need for a unique null device so "X = don't care" on the address lines RxAdr[4:0] can be any address between 0 and 31.

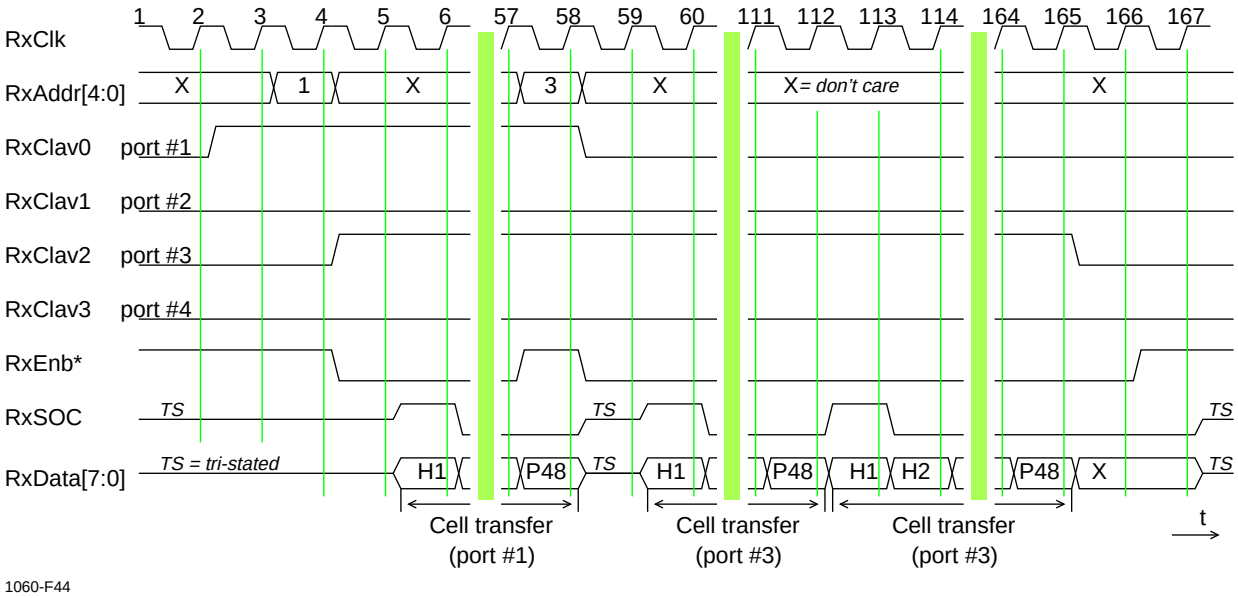


Figure 4.10. Example direct status indication, receive direction, 8-bit bus

In Figure 4.10 the polling of PHY ports starts while no cell transfer takes place. The ATM layer monitors all four status signals RxClav[3:0]. At clock edge #3 it detects a cell available at PHY port #1 (RxClav0 asserted). It selects that PHY port by placing address #1 on the address lines with rising clock edge #3. PHY port #1 detects this at clock edge #4. At clock edge #5 PHY port #1 detects RxEnb* asserted, thus cell transfer for PHY port #1 starts with rising clock edge #5. At clock edge #5 the ATM layer detects a cell available at PHY port #3 (RxClav2 asserted). Not knowing whether PHY port #1 may have another cell available or not, the ATM layer deselects PHY port #1 and selects PHY port #3 for cell transfer with rising clock edge #57 by placing address #3 on the address lines and deasserting RxEnb*. PHY port #1 and PHY port #3 detect this at clock edge #58. At clock edge #59 PHY port #3 detects RxEnb* asserted, thus cell transfer starts with rising clock edge #59. At clock edge #111 no cell is available at PHY ports #1, #2 and #4. The ATM layer keeps RxEnb* asserted and detects at clock edge #113 the first byte of another cell available from PHY port #3 (RxClav2 asserted). Thus, cell transfer takes place starting with rising clock edge #112. At clock edge #164, again, no cell is available at PHY ports #1, #2 and #4. The ATM layer keeps the RxEnb* asserted and detects at clock edge #166 also no cell available from PHY port #3 (RxClav2 deasserted). Thus, the ATM layer deselects PHY port #3 by deasserting RxEnb* with rising clock edge #166.

Figure 4.11 depicts the same case as Figure 4.10, except that PHY port #1 has priority. Thus, the ATM layer monitors always the PHY port #1 status signal prior to any other PHY port selection. The polling of PHY ports starts while no cell transfer takes place. The ATM layer monitors all four status signals RxClav[3:0]. At clock edge #3 it detects a cell available at PHY port #1

(RxClav0 asserted). It selects that PHY port by placing address #1 on the address lines with rising clock edge #3. PHY port #1 detects this at clock edge #4. At clock edge #5 PHY port #1 detects RxEnb* asserted, thus cell transfer for PHY port #1 starts with rising clock edge #5.

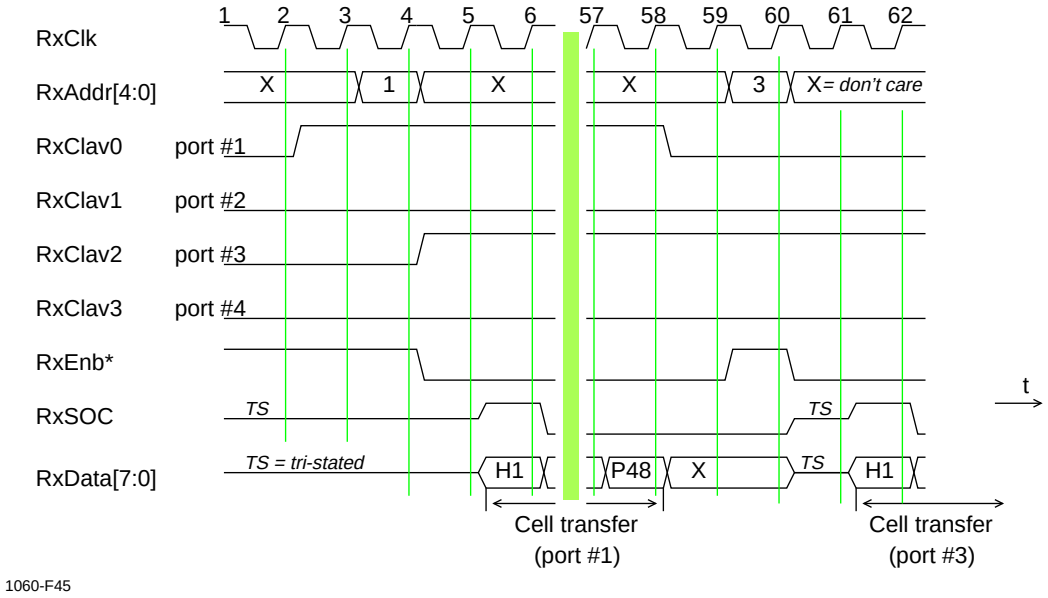


Figure 4.11. Example direct status indication, receive direction, 8-bit bus

At clock edge #5 the ATM layer detects a cell available at PHY port #3 (RxClav2 asserted). In contrast to Figure 4.10, with rising clock edge #57 the ATM layer does not deselect PHY port #1. In case another cell will be available from PHY port #1, this PHY port remains selected because RxEnb* remains asserted (analogous to Figure 4.10, clock edges #111...#114). At clock edge #59 the ATM layer detects no cell available from PHY port #1 (RxClav0 = deasserted). Thus, with rising clock edge #59 PHY port #3 is selected by placing address #3 on the address lines and deasserting RxEnb*. PHY port #1 and PHY port #3 detect this at clock edge #60. At clock edge #61 PHY port #3 detects RxEnb* asserted, thus cell transfer for PHY port #3 starts with rising clock edge #61.

In Figure 4.12 the polling of PHY ports starts while no cell transfer takes place. The ATM layer monitors all four status signals RxClav[3:0]. At clock edge #3 it detects a cell available at PHY port #1 (RxClav0 asserted). It selects that PHY port by placing address #1 on the address lines with rising clock edge #3. PHY port #1 detects this at clock edge #4. At clock edge #5 PHY port #1 detects RxEnb* asserted, thus cell transfer for PHY port #1 starts with rising clock edge #5.
At clock edge #5 the ATM layer detects a cell available at PHY port #3 (RxClav2 asserted). With rising clock edge #55 the ATM layer deasserts RxEnb* (ATM layer may suspend cell transfers at any time) and outputs address #1 on the address lines. At clock edge #56 the ATM layer detects a cell available at PHY port #2 (RxClav1 asserted). At clock edge #57 it is able to receive more bytes, thus with rising clock edge #57 it asserts RxEnb* again. No other PHY ports get selected due to address #1 on the address lines.

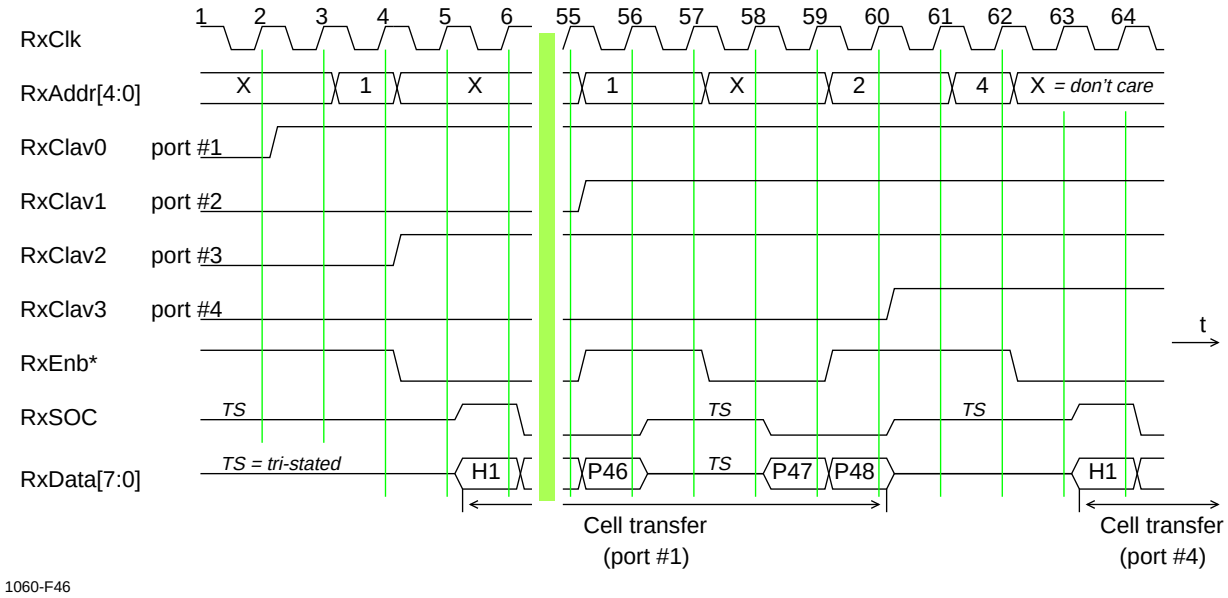


Figure 4.12. Example direct status indication, receive direction, 8-bit bus

With rising clock edge #59 the ATM layer deasserts RxEnb* for terminating this cell transfer. Simultaneously, the ATM layer has made the preliminary decision to select PHY port #2 as next (priority: 4>1>2>3), thus it outputs this address with rising clock edge #59. However, it does not select PHY port #2 until it has read the status from PHY port #1 (last cell transfer). In case PHY port #2 is finally selected, the ATM layer could assert RxEnb* already with rising clock edge #61. At clock edge #61 it detects RxClav0 (PHY port #1) and RxClav3 (PHY port #4) asserted. The highest priority is associated to PHY port #4, thus the ATM layer outputs address #4 with rising clock edge #61 and asserts RxEnb* with rising clock edge #62. PHY port #4 detects this at clock edges #62 and #63 respectively and starts cell transfer with rising clock edge #63.

4.3.2.2 Transmit direction

Examples for the transmit direction are given in Figure 4.13 and Figure 4.14. Signals TxClav[3:0] are associated to PHY port addresses #4, #3, #2 and #1, see Figure 4.3. Note, in principle any unique port address can be assigned to the four PHY ports. There is no need for a unique null device, thus "X = don't care" represents any address between 0 and 31 on the address lines TxAdr[4:0] or any data on the data bus.

In Figure 4.13 the polling of PHY ports starts while no cell transfer takes place. The ATM layer has pending cells for all four PHY ports (one individual queue for each PHY port) but all four PHY ports cannot accept a cell. With rising clock edge #2 PHY port #1 indicates that it can accept a complete cell (TxClav0 asserted). The ATM layer detects this at clock edge #3. It selects that PHY port by placing address #1 on the address lines with rising clock edge #3. PHY port #1 detects this at clock edge #4. At clock edge #5 PHY port #1 detects TxEnb* asserted, thus cell transfer for PHY port #1 starts with rising clock edge #5 (byte H1).

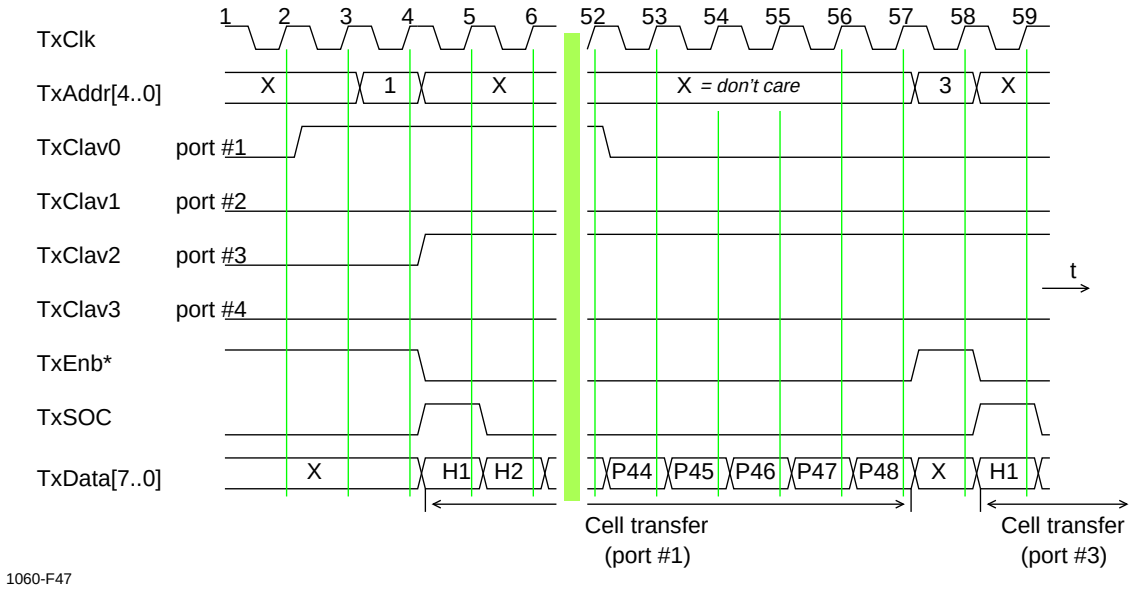


Figure 4.13. Example direct status indication, transmit direction, 8-bit bus

At clock edge #5 the ATM layer detects a cell available at PHY port #3 (TxClav2 asserted). With rising clock edge #52 PHY port #1 indicates that it cannot accept an additional cell by deasserting TxClav0. Thus, at clock edge #57 the ATM layer detects only TxClav2 asserted (TxClav1 and TxClav3 remain deasserted all the time). The ATM layer deselects PHY port #1 and selects PHY port #3 for cell transfer with rising clock edge #57 by placing address #3 on the address lines and deasserting TxEnb*. PHY port #1 and PHY port #3 detect this at clock edge #58. At clock edge #59 PHY port #3 detects TxEnb* asserted, thus cell transfer for PHY port #3 starts with rising clock edge #59 (byte H1).

In Figure 4.14 the polling of PHY ports starts while a cell transfer to PHY port #2 takes place. The ATM layer holds another pending cell for PHY port #2 and no pending cells for PHY ports 1, 3 and 4. With rising clock edge #1 PHY port #2 indicates that it cannot accept another cell (TxClav1 deasserted). The ATM layer detects this at clock edge #2. With rising clock edge #4 the ATM layer detects that PHY port #1 can accept a cell. With rising clock edge #5 PHY port #2 indicates that it can accept a next cell. The ATM layer detects this at clock edge #6, just in time before it would deassert TxEnb* at the end of the current cell transfer. Holding a cell pending for PHY port #2 at clock edge #6, the ATM layer just continues with the next cell transfer to PHY port #2 and outputs the first byte (byte H1) with rising clock edge #6. With rising clock edge #55 it suspends transmission for one clock cycle (the ATM layer may suspend cell transfers at any time). During the time period TxEnb* is deasserted, the ATM layer outputs the port address of the currently selected PHY port on the address lines TxAddr[4:0]. At clock edge #56 the ATM layer is able to transmit more bytes, thus with rising clock edge #56 it asserts TxEnb* again. No other PHY port is selected due to address #2 on the address lines.

At clock edge #60 there are no more pending cells. Thus, the ATM layer terminates the transfer by deasserting TxEnb* with rising clock edge #60.

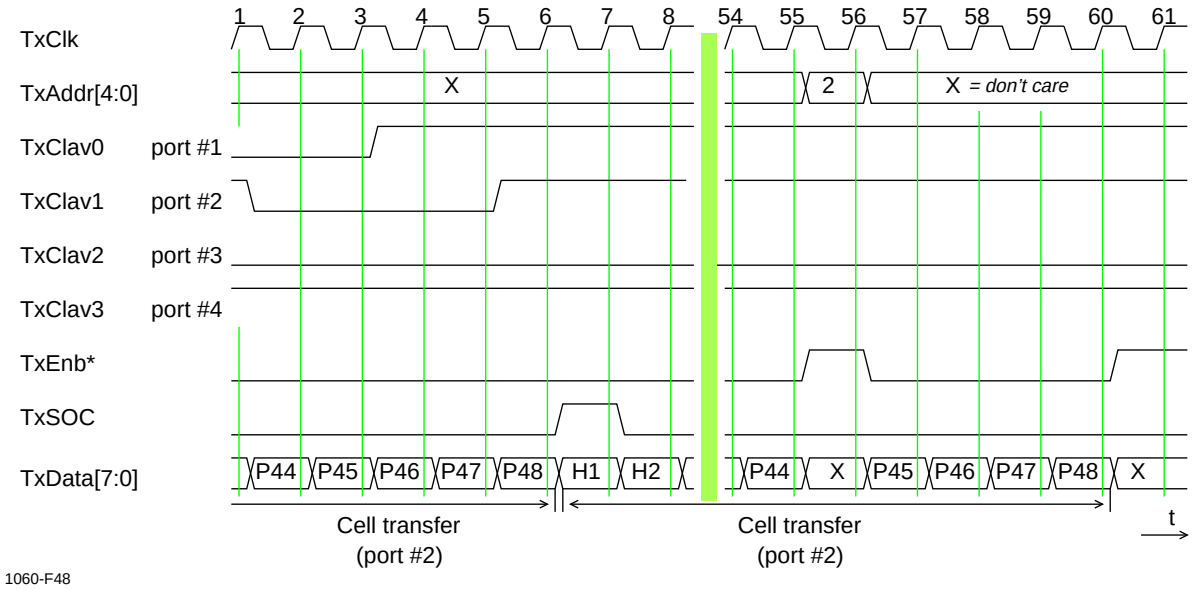


Figure 4.14. Example direct status indication, transmit direction, 8-bit bus

4.4 Multiplexed status polling

4.4.1 Method

Let us consider a maximum of 31 PHY ports connected to one ATM layer. Using the mechanism described in chapter 4.3, the status signals of four PHY ports are read simultaneously in one status poll cycle (receive direction: RxClav[3:0], transmit direction: TxClav[3:0]). Every PHY port address is allocated in a fixed manner to one of the four status signals of each direction and to one of eight PHY port groups. This allocation is defined in Table 4.1 and Table 4.2. For a given PHY port address the index [3:0] of the corresponding status signal can be derived by the two least significant bits of the PHY port address. The PHY port addresses are grouped together according to Table 4.2. The group number of a PHY port address can be derived by the three most significant bits of the PHY port address.

Note, the maximal number of PHY ports is 31 (31 PHY ports, port addresses #0...#30, and one null port, port address #31). Therefore, PHY port address #31 is not included in Table 4.1 and Table 4.2. The PHY port addresses for receive and transmit direction for one bi-directional PHY port are identical.

Table 4.1: PHY port address allocation

Signal	PHY port Address
RxClav0	0, 4, 8, 12, 16, 20, 24, 28
RxClav1	1, 5, 9, 13, 17, 21, 25, 29
RxClav2	2, 6, 10, 14, 18, 22, 26, 30
RxClav3	3, 7, 11, 15, 19, 23, 27
TxClav0	0, 4, 8, 12, 16, 20, 24, 28
TxClav1	1, 5, 9, 13, 17, 21, 25, 29
TxClav2	2, 6, 10, 14, 18, 22, 26, 30
TxClav3	3, 7, 11, 15, 19, 23, 27

Table 4.2: PHY Port Address Allocation to Group Address

PHY Port Address	Group Number	Group Number on Addr[4:0]
0, 1, 2, 3	0	000 xx
4, 5, 6, 7	1	001 xx
8, 9, 10, 11	2	010 xx
12, 13, 14, 15	3	011 xx
16, 17, 18, 19	4	100 xx
20, 21, 22, 23	5	101 xx
24, 25, 26, 27	6	110 xx
28, 29, 30	7	111 0x, 111 10

x = don’t care

In order to poll the status of PHY ports, the ATM layer places a group address left adjusted on the address lines Addr[4:0], see Table 4.2. All PHY ports of that considered group respond via the correspondent status signal RxClav (receive direction) or TxClav (transmit direction). The ATM layer knows the existing PHY ports and masks out status signals not used in a poll cycle. PHY port address 31 addresses the null device and is not a member of a group. No PHY device responds in any case if PHY port address 31 is placed on the address bus. This allows various PHY device implementations as long as the defined allocation rule is followed.

4.4.2 Example

4.4.2.1 ATM/PHY layer interconnection

In Figure 4.15 an example for eight PHY devices is shown. Each device has one PHY port. The numbering of the PHY devices and PHY ports from 1 to 8 is arbitrary and has no impact on the addressing scheme. In principle, there is no relationship between PHY port number and PHY port address. To each PHY port one unique PHY port address has been assigned (by configuration, management interface) according to the status signal the PHY device is connected to. The figure shows two examples of this PHY port address assignment (two rows “port address”). In general:

- PHY device #1 is connected to RxClav0/TxClav0 and its PHY port may have one port address out of [0, 4, 8, 12, 16, 20, 24, 28]
- PHY device #2 is connected to RxClav1/TxClav1 and its PHY port may have one port address out of [1, 5, 9, 13, 17, 21, 25, 29]

- PHY device #7 is connected to RxClav2/TxClav2 and its PHY port may have one port address out of [2, 6, 10, 14, 18, 22, 26, 30]
- PHY device #8 is connected to RxClav3/TxClav3 and its PHY port may have one port address out of [3, 7, 11, 15, 19, 23, 27].

1060-F49

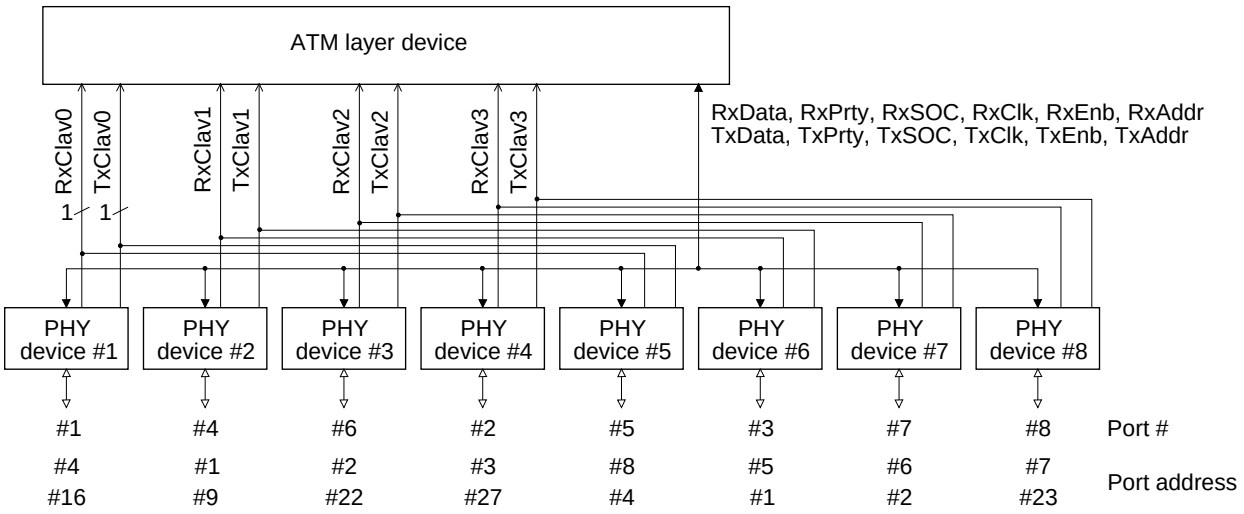


Figure 4.15. Example multiplexed status polling, 8 PHY devices, one PHY port per device

In Figure 4.16 (transmit direction) and Figure 4.17 (receive direction) two examples for 8 PHY devices and 31 PHY ports are shown. Each device has four PHY ports and four status signals. Note, in Figure 4.16 only one PHY device responds to a poll cycle, driving all its four status signals (except for PHY device #8, group #7). In Figure 4.17 four PHY devices respond simultaneously to a poll cycle, each driving one status signal (except for group #7).

1060F410

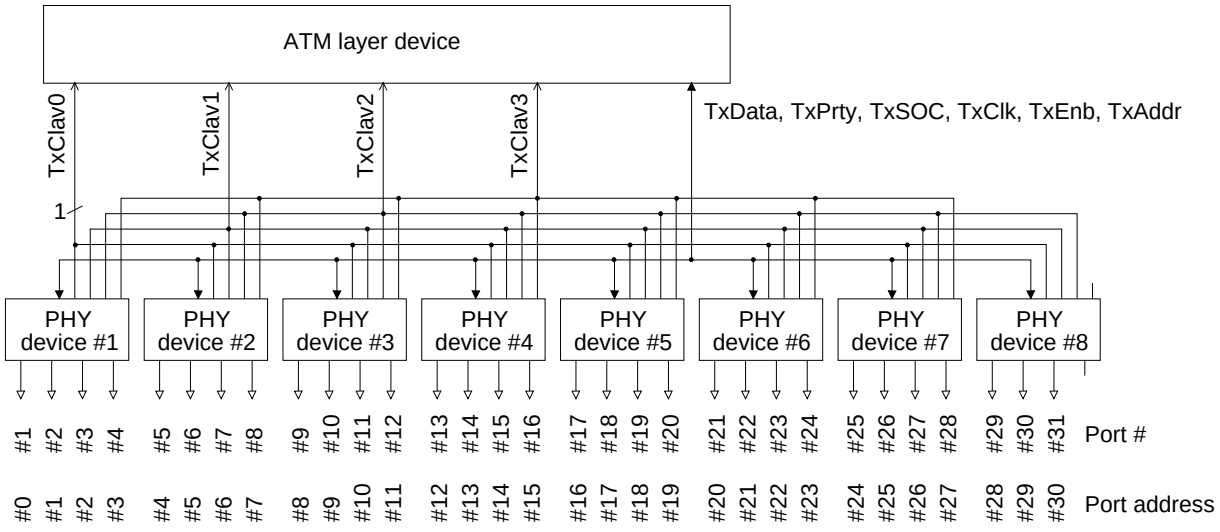


Figure 4.16. Example multiplexed status polling, 8 PHY devices, 4 PHY ports per device

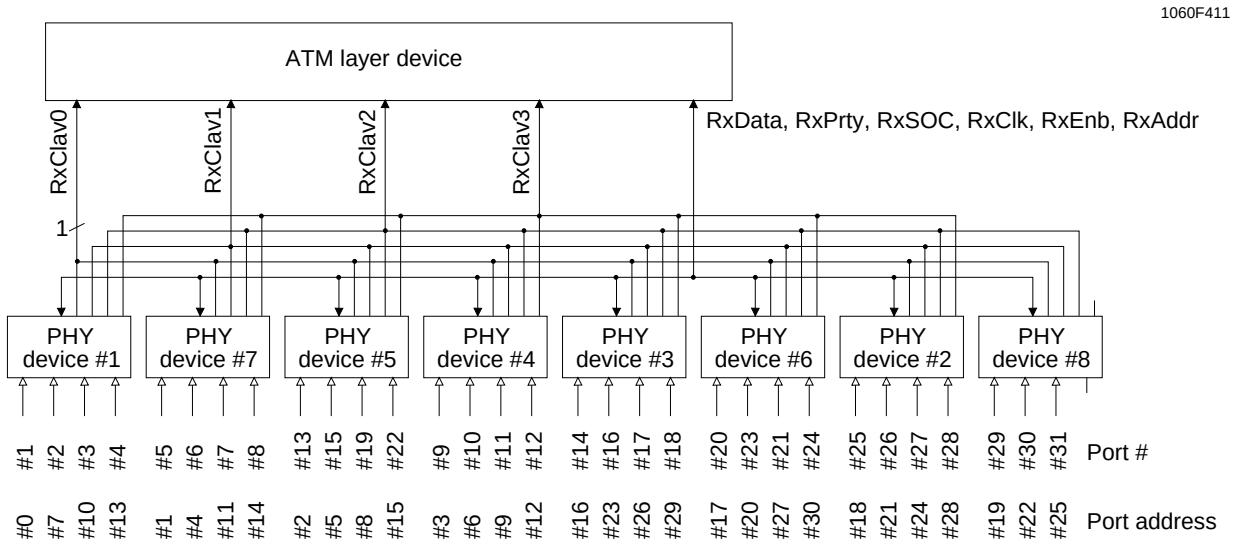


Figure 4.17. Example multiplexed status polling, 8 PHY devices, 4 PHY ports per device

Figure 4.18 shows an example (transmit direction) for four PHY devices, 31 PHY ports, 8 PHY ports per device and each PHY device with only one status signal per direction. Except for group #7, four PHY devices respond simultaneously to a poll cycle.

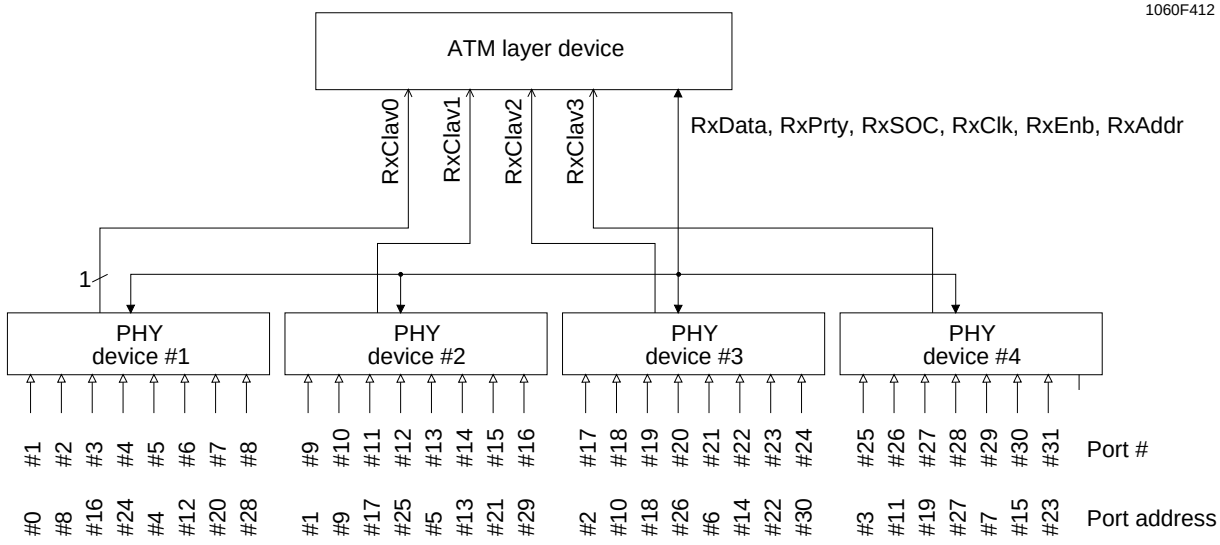


Figure 4.18. Example multiplexed status polling, 4 PHY devices, 8 PHY ports per device

4.4.2.2 Timing

Figure 4.19 shows an example (receive direction) for the timing of four multiplexed status signals. Status polling starts during a cell transfer from PHY port #14. The ATM layer polls four PHY ports in parallel. It selects group #5 by placing address #20 on the address lines with rising clock edge #1 and deselects it again with rising clock edge #2. Group #5 (PHY ports #20, #21, #22 and #23) detects being addressed at clock edge #2 and outputs its status with rising clock edge #2. This status is read by the ATM layer at clock edge #3 (note: the address of the null PHY port is #31).

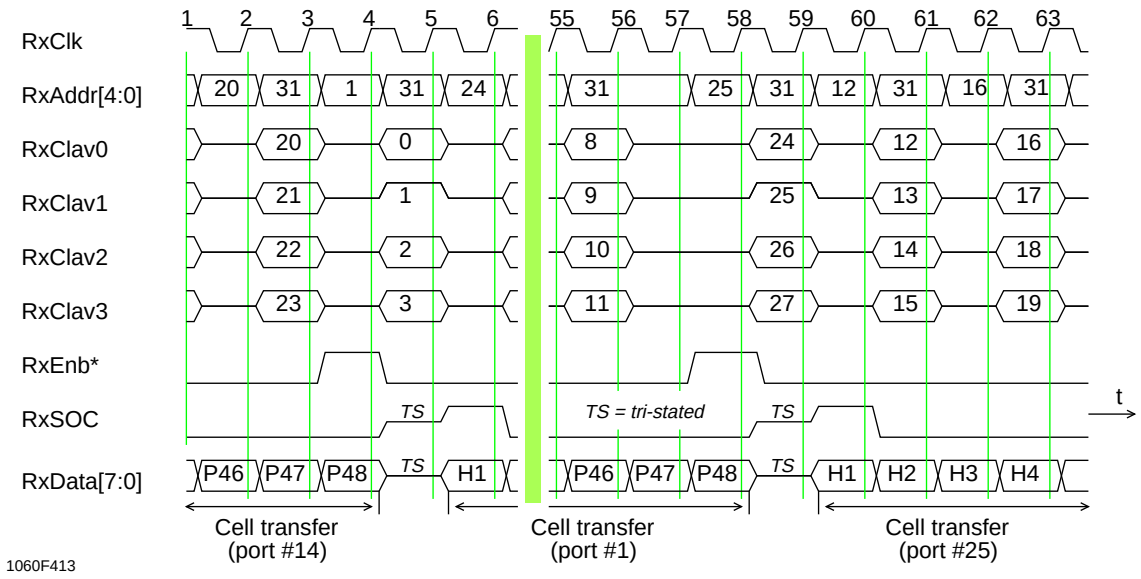


Figure 4.19. Example multiplexed status polling, receive direction

At clock edge #4 the current cell transfer terminates. With rising clock edge #3 the ATM layer suspends the polling of PHY ports and selects PHY port #1 as next for cell transfer. With rising clock edge #5 it resumes polling by placing the next group address on the address lines.

Note, PHY port address #1 at clock edge #4 is primarily used for selecting that PHY port for cell transfer (RxEnb* deasserted). For the polling mechanism it looks like a regular poll for group #0. Thus, PHY ports #0, #1, #2, and #3 respond and drive the status signals with rising clock edge #4. This status is read by the ATM layer at clock edge #5.

With rising clock edge #54, the ATM layer selects group #2 by placing address #8 on the address lines and deselects it again with rising clock edge #55. Group #2 (PHY ports #8, #9, #10 and #11) detects being addressed at clock edge #55 and outputs its status with rising clock edge #55. This status is read by the ATM layer at clock edge #56.

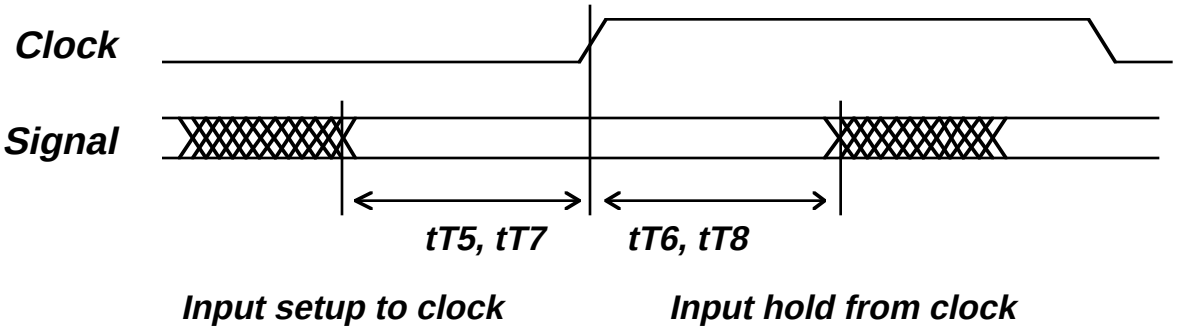
At clock edge #58 the current cell transfer terminates. Thus, at clock edges #56 and #57 the ATM layer suspends the polling for two clock cycles. This ensures that cell transfers are back to back without a second unused clock cycle. PHY port #25 is selected at clock edge #58 and polling is resumed by placing the next group address on the address lines with rising clock edge #58. At clock edge #59 the ATM layer reads the status of group #6.

Let us consider the ATM layer suspends cell transmission during a cell transfer (the ATM layer may suspend cell transfer at any time). The ATM layer may continue to poll the status while the cell transfer is suspended. To resume cell transfer, the ATM layer must resume and place the appropriate PHY port address on the address lines, see also Figure 4.12.

5. Timing Details at 25, 33 and 50 MHz

5.1 A.C. characteristics

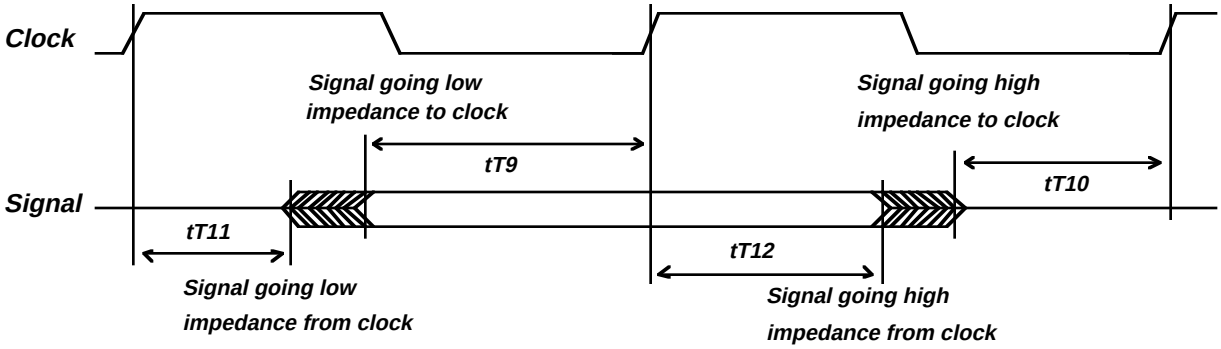
The A.C. characteristics are based on the timing specification for the receiver side of a signal. The setup and the hold times are defined with regard to a positive clock edge, see Figure 5.1. Taking the actual used clock frequency into account (e.g. up to the max. frequency), the corresponding (min. and max.) transmit side "clock to output" propagation delay specifications can be derived. The timing references (tT5 to tT12) are according to tables 5.1 to 5.16.



1062-F1

Figure 5.1: Setup and hold time definition (single- and multi-PHY)

Figure 5.2 shows the tri-state timing for the multi-PHY application (multiple PHY devices, multiple output signals are multiplexed together).



1062-F2

Figure 5.2: Tri-state timing (multi-PHY, multiple devices only)

In the following tables, A⇒P (column DIR, Direction) defines a signal from the ATM layer (transmitter, driver) to the PHY layer (receiver), A⇐P defines a signal from the PHY layer (transmitter, driver) to the ATM layer (receiver).
The signals TxRef* and RxRef* are not included in the A.C. characteristics, see also chapter 5.3.

5.1.1 8-bit data bus (Û155 Mbps line rate), single-PHY

Note: There are no tri-stated signals. Common A.C. parameters are listed in chapter 5.1.9.

5.1.1.1 Transmit Direction

Table 5.1: Transmit timing (8-bit data bus, Û155Mbps line rate, single-PHY)

Signal name	DIR	Item	Description	Min.	Max.
TxClk	A⇒P	f1	TxClk frequency (nominal)	0	25MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	4ns
TxData[7:0], TxPrty, TxSOC, TxEnb*	A⇒P	tT5	Input setup to TxClk	10ns	-
		tT6	Input hold from TxClk	1ns	-
TxFull*/TxClav	A⇐P	tT7	Input setup to TxClk	10ns	-
		tT8	Input hold from TxClk	1ns	-

5.1.1.2 Receive Direction

Table 5.2: Receive timing (8-bit data bus, Û155 Mbps line rate, single-PHY)

Signal name	DIR	Item	Description	Min.	Max.
RxClk	A⇒P	f1	RxClk frequency (nominal)	0	25MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	4ns
RxEnb*	A⇒P	tT5	Input setup to RxClk	10ns	-
		tT6	Input hold from RxClk	1ns	-
RxData[7:0], RxPrty, RxSOC, RxEmpty*/RxClav	A⇐P	tT7	Input setup to RxClk	10ns	-
		tT8	Input hold from RxClk	1ns	-

5.1.2 8-bit data bus (Û33 MHz at cell interface), single-PHY

Note: There are no tri-stated signals. Common A.C. parameters are listed in chapter 5.1.9.

5.1.2.1 Transmit Direction

Table 5.3: Transmit timing (8-bit data bus, Û33 MHz at cell interface, single-PHY)

Signal name	DIR	Item	Description	Min.	Max.
TxClk	A⇒P	f1	TxClk frequency (nominal)	0	33MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	3ns
TxData[7:0], TxPrty, TxSOC, TxEnb*	A⇒P	tT5	Input setup to TxClk	8ns	-
		tT6	Input hold from TxClk	1ns	-
TxFull*/TxClav	A⇐P	tT7	Input setup to TxClk	8ns	-
		tT8	Input hold from TxClk	1ns	-

5.1.2.2 Receive Direction

Table 5.4: Receive timing (8-bit data bus, Û33 MHz at cell interface, single-PHY)

Signal name	DIR	Item	Description	Min.	Max.
RxClk	A⇒P	f1	RxClk frequency (nominal)	0	33MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	3ns
RxEnb*	A⇒P	tT5	Input setup to RxClk	8ns	-
		tT6	Input hold from RxClk	1ns	-
RxData[7:0], RxPrty, RxSOC, RxEmpty*/RxClav	A⇐P	tT7	Input setup to RxClk	8ns	-
		tT8	Input hold from RxClk	1ns	-

5.1.3 16-bit data bus (Û33 MHz at cell interface), single-PHY

Note: There are no tri-stated signals. Common A.C. parameters are listed in chapter 5.1.9.

5.1.3.1 Transmit Direction

Table 5.5: Transmit timing (16-bit data bus, Û33 MHz at cell interface, single-PHY)

Signal name	DIR	Item	Description	Min.	Max.
TxClk	A⇒P	f1	TxClk frequency (nominal)	0	33MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	3ns
TxData[15:0], TxPrty, TxSOC, TxEnb*	A⇒P	tT5	Input setup to TxClk	8ns	-
		tT6	Input hold from TxClk	1ns	-
TxFull*/TxClav	A⇐P	tT7	Input setup to TxClk	8ns	-
		tT8	Input hold from TxClk	1ns	-

5.1.3.2 Receive Direction

Table 5.6: Receive timing (16-bit data bus, Û33 MHz at cell interface, single-PHY)

Signal name	DIR	Item	Description	Min.	Max.
RxClk	A⇒P	f1	RxClk frequency (nominal)	0	33MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	3ns
RxEnb*	A⇒P	tT5	Input setup to RxClk	8ns	-
		tT6	Input hold from RxClk	1ns	-
RxData[15:0], RxPrty, RxSOC, RxEmpty*/RxClav	A⇐P	tT7	Input setup to RxClk	8ns	-
		tT8	Input hold from RxClk	1ns	-

5.1.4 16-bit data bus (Û50 MHz at cell interface), single-PHY

Note: There are no tri-stated signals. Common A.C. parameters are listed in chapter 5.1.9.

5.1.4.1 Transmit Direction

Table 5.7: Transmit timing (16-bit data bus, Û50 MHz at cell interface, single-PHY)

Signal name	DIR	Item	Description	Min.	Max.
TxClk	A⇒P	f1	TxClk frequency (nominal)	0	50MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	2ns
TxData[15:0], TxPrty, TxSOC, TxEnb*	A⇒P	tT5	Input setup to TxClk	4ns	-
		tT6	Input hold from TxClk	1ns	-
TxFull*/TxClav	A⇐P	tT7	Input setup to TxClk	4ns	-
		tT8	Input hold from TxClk	1ns	-

5.1.4.2 Receive Direction

Table 5.8: Receive timing (16-bit data bus, Û50 MHz at cell interface, single-PHY)

Signal name	DIR	Item	Description	Min.	Max.
RxClk	A⇒P	f1	RxClk frequency (nominal)	0	50MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	2ns
RxEnb*	A⇒P	tT5	Input setup to RxClk	4ns	-
		tT6	Input hold from RxClk	1ns	-
RxData[15:0], RxPrty, RxSOC, RxEmpty*/RxClav	A⇐P	tT7	Input setup to RxClk	4ns	-
		tT8	Input hold from RxClk	1ns	-

5.1.5 8-bit data bus (Û155 Mbps line rate), multi-PHY

Note: Common A.C. parameters are listed in chapter 5.1.9. Notes (1), (2) are listed in chapter 5.2.5.

5.1.5.1 Transmit Direction

Table 5.9: Transmit timing (8-bit data bus, Û155 Mbps line rate, multi-PHY)

Signal name	DIR	Item	Description	Min.	Max.
TxClk	A⇒P	f1	TxClk frequency (nominal)	0	25MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	4ns
TxData[7:0], TxPrty, TxSOC, TxEnb*, TxAddr[4:0]	A⇒P	tT5	Input setup to TxClk	10ns	-
		tT6	Input hold from TxClk	1ns	-
TxFull*/TxClav [3:0]	A⇐P	tT7	Input setup to TxClk	10ns	-
		tT8	Input hold from TxClk	1ns	-
		tT9	Signal going low impedance to TxClk	10ns	-
		tT10	Signal going high impedance to TxClk (1)	0ns	-
		tT11	Signal going low impedance from TxClk	1ns	-
		tT12	Signal going high impedance from TxClk	1ns	-

5.1.5.2 Receive Direction

Table 5.10: Receive timing (8-bit data bus, Û155 Mbps line rate, multi-PHY)

Signal name	DIR	Item	Description	Min.	Max.
RxClk	A⇒P	f1	RxClk frequency (nominal)	0	25MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	RxClk rise/fall time	-	4ns
RxEnb*, RxAddr[4:0]	A⇒P	tT5	Input setup to RxClk	10ns	-
		tT6	Input hold from RxClk	1ns	-
RxData[7:0], RxPrty, RxSOC, RxEmpty*/RxClav [3:0]	A⇐P	tT7	Input setup to RxClk	10ns	-
		tT8	Input hold from RxClk	1ns	-
		tT9	Signal going low impedance to RxClk	10ns	-
		tT10	Signal going high impedance to RxClk (2)	0ns	-
		tT11	Signal going low impedance from RxClk	1ns	-
		tT12	Signal going high impedance from RxClk	1ns	-

5.1.6 8-bit data bus (Û33 MHz at cell interface), multi-PHY

Note: Common A.C. parameters are listed in chapter 5.1.9. Notes (1), (2) are listed in chapter 5.2.5.

5.1.6.1 Transmit Direction

Table 5.11: Transmit timing (8-bit data bus, Û33 MHz at cell interface, multi-PHY)

Signal name	DIR	Item	Description	Min.	Max.
TxClk	A⇒P	f1	TxClk frequency (nominal)	0	33MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	3ns
TxData[7:0], TxPrty, TxSOC, TxEnb*, TxAddr[4:0]	A⇒P	tT5	Input setup to TxClk	8ns	-
		tT6	Input hold from TxClk	1ns	-
TxFull*/TxClav [3:0]	A⇐P	tT7	Input setup to TxClk	8ns	-
		tT8	Input hold from TxClk	1ns	-
		tT9	Signal going low impedance to TxClk	8ns	-
		tT10	Signal going high impedance to TxClk (1)	0ns	-
		tT11	Signal going low impedance from TxClk	1ns	-
		tT12	Signal going high impedance from TxClk	1ns	-

5.1.6.2 Receive Direction

Table 5.12: Receive timing (8-bit data bus, Û33 MHz at cell interface, multi-PHY)

Signal name	DIR	Item	Description	Min.	Max.
RxClk	A⇒P	f1	RxClk frequency (nominal)	0	33MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	RxClk rise/fall time	-	3ns
RxEnb*, RxAddr[4:0]	A⇒P	tT5	Input setup to RxClk	8ns	-
		tT6	Input hold from RxClk	1ns	-
RxData[7:0], RxPrty, RxSOC, RxEmpty*/RxClav [3:0]	A⇐P	tT7	Input setup to RxClk	8ns	-
		tT8	Input hold from RxClk	1ns	-
		tT9	Signal going low impedance to RxClk	8ns	-
		tT10	Signal going high impedance to RxClk (2)	0ns	-
		tT11	Signal going low impedance from RxClk	1ns	-
		tT12	Signal going high impedance from RxClk	1ns	-

5.1.7 16-bit data bus (Û33 MHz at cell interface), multi-PHY

Note: Common A.C. parameters are listed in chapter 5.1.9. Notes (1), (2) are listed in chapter 5.2.5.

5.1.7.1 Transmit Direction

Table 5.13: Transmit timing (16-bit data bus, Û33 MHz at cell interface, multi-PHY)

Signal name	DIR	Item	Description	Min.	Max.
TxClk	A⇒P	f1	TxClk frequency (nominal)	0	33MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	3ns
TxData[15:0], TxPrty, TxSOC, TxEnb*, TxAddr[4:0]	A⇒P	tT5	Input setup to TxClk	8ns	-
		tT6	Input hold from TxClk	1ns	-
TxFull*/TxClav [3:0]	A⇐P	tT7	Input setup to TxClk	8ns	-
		tT8	Input hold from TxClk	1ns	-
		tT9	Signal going low impedance to TxClk	8ns	-
		tT10	Signal going high impedance to TxClk (1)	0ns	-
		tT11	Signal going low impedance from TxClk	1ns	-
		tT12	Signal going high impedance from TxClk	1ns	-

5.1.7.2 Receive Direction

Table 5.14: Receive timing (16-bit data bus, Û33 MHz at cell interface, multi-PHY)

Signal name	DIR	Item	Description	Min.	Max.
RxClk	A⇒P	f1	RxClk frequency (nominal)	0	33MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	RxClk rise/fall time	-	3ns
RxEnb*, RxAddr[4:0]	A⇒P	tT5	Input setup to RxClk	8ns	-
		tT6	Input hold from RxClk	1ns	-
RxData[15:0], RxPrty, RxSOC, RxEmpty*/RxClav [3:0]	A⇐P	tT7	Input setup to RxClk	8ns	-
		tT8	Input hold from RxClk	1ns	-
		tT9	Signal going low impedance to RxClk	8ns	-
		tT10	Signal going high impedance to RxClk (2)	0ns	-
		tT11	Signal going low impedance from RxClk	1ns	-
		tT12	Signal going high impedance from RxClk	1ns	-

5.1.8 16-bit data bus (Û50 MHz at cell interface), multi-PHY

Note: Common A.C. parameters are listed in chapter 5.1.9. Notes (1), (2) are listed in chapter 5.2.5.

5.1.8.1 Transmit Direction

Table 5.15: Transmit timing (16-bit data bus, Û50 MHz at cell interface, multi-PHY)

Signal name	DIR	Item	Description	Min.	Max.
TxClk	A⇒P	f1	TxClk frequency (nominal)	0	50MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	2ns
TxData[15:0], TxPrty, TxSOC, TxEnb*, TxAddr[4:0]	A⇒P	tT5	Input setup to TxClk	4ns	-
		tT6	Input hold from TxClk	1ns	-
TxFull*/TxClav [3:0]	A⇐P	tT7	Input setup to TxClk	4ns	-
		tT8	Input hold from TxClk	1ns	-
		tT9	Signal going low impedance to TxClk	4ns	-
		tT10	Signal going high impedance to TxClk (1)	0ns	-
		tT11	Signal going low impedance from TxClk	1ns	-
		tT12	Signal going high impedance from TxClk	1ns	-

5.1.8.2 Receive Direction

Table 5.16: Receive timing (16-bit data bus, Û50 MHz at cell interface, multi-PHY)

Signal name	DIR	Item	Description	Min.	Max.
RxClk	A⇒P	f1	RxClk frequency (nominal)	0	50MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	RxClk rise/fall time	-	2ns
RxEnb*, RxAddr[4:0]	A⇒P	tT5	Input setup to RxClk	4ns	-
		tT6	Input hold from RxClk	1ns	-
RxData[15:0], RxPrty, RxSOC, RxEmpty*/RxClav [3:0]	A⇐P	tT7	Input setup to RxClk	4ns	-
		tT8	Input hold from RxClk	1ns	-
		tT9	Signal going low impedance to RxClk	4ns	-
		tT10	Signal going high impedance to RxClk (2)	0ns	-
		tT11	Signal going low impedance from RxClk	1ns	-
		tT12	Signal going high impedance from RxClk	1ns	-

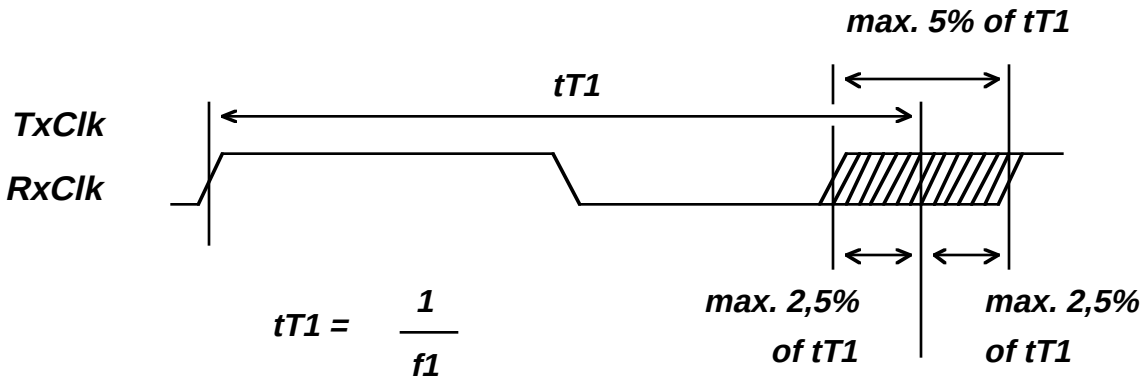
5.1.9 Common parameters for A.C. characteristics

Table 5.17 lists the common parameters for the A.C. characteristics. Notes (3), (15), (16) are listed in chapter 5.2.5.

Table 5.17: Common parameters for A.C. characteristics

Parameter	Typ.	Min.	Max.
Input capacitance of input or input/output signal (pin)	10pF	-	
Input and output timing reference level	1.4V	-	-
Temperature range (Tambient) (15)	-	0 to +70ßC	-
Power supply VDD (3)	+5V or +3,3V	-	-
Power supply Tolerance (16)	-	Ò5%	-

RxClk and TxClk peak-to-peak jitter, (for one cycle)	measured from one rising edge to the next rising edge
RxClk and TxClk rise time	measured at transmit side (driver), unloaded measured between 10% and 90% levels of VOH
RxClk and TxClk fall time	measured at transmit side (driver), unloaded measured between 90% and 10% levels of VOH



1062-F3

Figure 5.3: Clock peak-to-peak jitter

5.2 D.C. characteristics

The following chapters 5.2.1 and 5.2.2 list the D.C. characteristics for the transmit and receive side of any single- or multi-PHY signal. The parameters assume, that all the PHY and ATM layer devices are located close to each other, minimizing transmission line effects.

5.2.1 Single-PHY configuration

D.C. characteristics of a single-PHY configuration (ATM layer intended for 155 Mbps or 622 Mbps line rate). Common D.C. characteristics are listed in chapter 5.2.4. Notes (4) to (10) are listed in chapter 5.2.5.

Table 5.18: D.C. characteristics (single-PHY, 155 Mbps, 622 Mbps)

Symbol	Parameter	Min.	Max.	Conditions
VIL	Input LOW voltage	-0,3V	+0.8V	(4)
VIH	Input HIGH voltage	+2.0V	VDD + 0.3V	(5)
VOH	Output or bi-directional HIGH voltage	+2.4V	-	IOH ≥ |-4mA| (6)
VOL	Output or bi-directional LOW voltage	-	+0,5V	IOL ≥ +4mA (7)
IOH	Output current at HIGH voltage	-4mA	-	VOH ≥ +2.4V (8)
IOL	Output current at LOW voltage	+4mA	-	VOL ≤ +0.5V (9)
IIH	Input current at HIGH voltage	-	-	(10)
IIL	Input current at LOW voltage	-	-	(10)

5.2.2 Multi-PHY configuration

5.2.2.1 ATM layer intended for ≤155 Mbps

D.C. characteristics of a multi-PHY configuration (ATM layer intended for ≤155 Mbps line rate). Common D.C. characteristics are listed in chapter 5.2.4. Notes (4), (5) (10) to (14) are listed in chapter 5.2.5.

Table 5.19: D.C. characteristics (multi-PHY, ≤155 Mbps)

Symbol	Parameter	Min.	Max.	Conditions
VIL	Input LOW voltage	-0,3V	+0.8V	(4)
VIH	Input HIGH voltage	+2.0V	VDD + 0.3V	(5)
VOH	Output or bi-directional HIGH voltage	+2.4V	-	IOH ≥ |-8mA| (11)
VOL	Output or bi-directional LOW voltage	-	+0,5V	IOL ≥ +8mA (12)
IOH	Output current at HIGH voltage	-8mA	-	VOH ≥ +2.4V (13)
IOL	Output current at LOW voltage	+8mA	-	VOL ≤ +0.5V (14)
IIH	Input current at HIGH voltage	-	-	(10)
IIL	Input current at LOW voltage	-	-	(10)

5.2.3 ATM layer intended for 622 Mbps

D.C. characteristics of a multi-PHY configuration (ATM layer intended for 622 Mbps line rate). Common D.C. characteristics are listed in chapter 5.2.4. Notes (4), (5), (10) to (14) are listed in chapter 5.2.5.

Table 5.20: D.C. characteristics (multi-PHY, 622Mbps)

Symbol	Parameter	Min.	Max.	Conditions
VIL	Input LOW voltage	-0,3V	+0.8V	(4)
VIH	Input HIGH voltage	+2.0V	VDD + 0.3V	(5)
VOH	Output or bi-directional HIGH voltage	+2.4V	-	IOH ≥ |-8mA| (11)
VOL	Output or bi-directional LOW voltage	-	+0,5V	IOL ≥ +8mA (12)
IOH	Output current at HIGH voltage	-8mA	-	VOH ≥ +2.4V (13)
IOL	Output current at LOW voltage	+8mA	-	VOL ≤ +0.5V (14)
IIH	Input current at HIGH voltage	-	-	(10)
IIL	Input current at LOW voltage	-	-	(10)

5.2.4 Common parameters for D.C. characteristics

Table 5.21 lists the common parameters for the D.C. characteristics. Notes (3), (15), (16) are listed in chapter 5.2.5.

Table 5.21: Common parameters for D.C. characteristics

Parameter	Typ.	Min.	Max.
Temperature range (Tambient) (15)	-	0 to +70ßC	-
Power supply VDD (3)	+5V or +3,3V	-	-
Power supply Tolerance (16)	-	Ò5%	-

5.2.5 Notes

(1) This gives one clock period time for the driver to switch in the high impedance state (signal going high impedance 0ns *in front of next* TxClk).

(2) This gives one clock period time for the driver to switch in the high impedance state (signal going high impedance 0ns *in front of next* RxClk).

(3) This specification defines either VDD = +5V or VDD = +3,3V. It assumes the same VDD on the transmit and receive side of a signal. It does not consider a mixed VDD (+5V/+3,3V) configuration.

(4) A device with VIL, min. ≤ -0.3V is compliant to this specification.

(5) A device with VIH, max. ≥ VDD+0.3V is compliant to this specification.

(6) Negative current flows out of the considered node (out of the PHY/ATM layer device pin). A device with VOH, min. ≥ +2.4V (and IOH ≥ |-4mA|) is compliant to this specification.

(7) Positive current flows into the considered node (into the PHY/ATM layer device pin). A device with VOL, max. ≤ +0.5V (and IOL ≥ +4mA) is compliant to this specification.

(8) Negative current flows out of the considered node (out of the PHY/ATM layer device pin). IOH, min. defines the minimal required IOH value for the driver.
A device with IOH, min. ≥ |-4mA| (and VOH ≥ +2.4V) is compliant to this specification.

(9) Positive current flows into the considered node (into the PHY/ATM layer device pin). IOL, min. defines the minimal required IOL value for the driver.
A device with IOL, min. ≥ +4mA (and VOL ≤ +0,5V) is compliant to this specification.

(10) To allow several technologies, no values for IIH and IIL are specified. An input can sink and source.

(11) Negative current flows out of the considered node (out of the PHY/ATM layer device pin).
A device with VOH, min. ≥ +2.4V (and IOH ≥ |-8mA|) is compliant to this specification.
(12) Positive current flows into the considered node (into the PHY/ATM layer device pin). A device with VOL, max. ≤ +0.5V (and IOL ≥ +8mA) is compliant to this specification.
(13) Negative current flows out of the considered node (out of the PHY/ATM layer device pin). IOH, min. defines the minimal required IOH value for the driver.
A device with IOH, min. ≥ |-8mA| (and VOH ≥ +2.4V) is compliant to this specification.
(14) Positive current flows into the considered node (into the PHY/ATM layer device pin). IOL, min. defines the minimal required IOL value for the driver.
A device with IOL, min. ≥ +8mA (and VOL ≤ +0,5V) is compliant to this specification.
(15) A device with a temperature range of at least 0 to +70ßC is compliant to this specification.
(16) A device with a power supply voltage tolerance ≥ 5% is compliant to this specification.

5.3 Signals TxRef* and RxRef*

In the UTOPIA level 1 document (V2.01), the signals TxRef* and RxRef* are defined as follows:

- Transmit Reference (TxRef*)
  Input to the PHY layer for synchronization purposes (e.g. 8kHz marker, frame indicator, etc.)
- Receive Reference (RxRef*)
  Output from the PHY layer for synchronization purposes (e.g. 8kHz marker, frame indicator, etc.).

Both signals deal direct with and depend on the chosen line interface type (e.g. SONET/SDH, cell based etc.). The ATM layer must always assume, these signals have no correlation to any other Utopia interface signal. Thus, TxRef* and RxRef* are not included in the A.C. characteristics (timing tables) of this document.

6. Data Path Signal Summary

This is a complete signal list for both transmit and receive data paths.

6.1. Transmit Interface Signals

Table 6.1. Transmit Interface Signals

Signal	Direction	Req./Opt	Description
TxAddr[4:0]	ATM to PHY	R for MPHY	Address of MPHY device being selected
TxData[7:0]	ATM to PHY	R	Data bus
TxData[15:8]	ATM to PHY	O	Data bus extension for 16-bit mode
TxPrty	ATM to PHY	O	Data bus odd parity
TxSOC	ATM to PHY	R	Start Of Cell
TxEnb*	ATM to PHY	R	Enable data transfers
TxFull*/ TxClav	PHY to ATM	R	FIFO full/Cell Buffer Available
TxClav[3..1]	PHY to ATM	O	Extra FIFO full/Cell Buffer Available
TxClk	ATM to PHY	R	Transfer/interface byte clock
TxRef*	ATM to PHY	O	Reference (e.g. 8 kHz)

6.2. Receive Interface Signals

Table 6.2. Receive Interface Signals

Signal	Direction	Req./Opt	Description
RxAddr[4:0]	ATM to PHY	R for MPHY	Address of MPHY device being selected
RxData[7:0]	PHY to ATM	R	Data bus
RxData[15:8]	PHY to ATM	O	Data bus extension for 16-bit mode
RxPrty	PHY to ATM	O	Data bus odd parity
RxSOC	PHY to ATM	R	Start Of Cell
RxEnb*	ATM to PHY	R	Enable data transfers
RxEmpty*/ RxClav	PHY to ATM	R	FIFO empty/Cell Available
RxClav[3..1]	PHY to ATM	O	Extra FIFO full/Cell Buffer Available
RxClk	ATM to PHY	R	Transfer/interface byte clock
RxRef*	PHY to ATM	O	Reference (e.g. 8 kHz)

Appendix 1. Method to support a larger number of PHYs

Using 2-cycle polls a maximum of 26 PHYs can be polled during the transmission time of one cell. This appendix describes a method for cases where more than 26 PHYs are connected to one ATM via the addition of optional Clav/Enb* signal pairs to the ATM. The ATM and PHY layers are not required to implement this appendix to be compliant with the Level 2 Utopia Specification.

A1.1. Example

In this example for the Receive interface the ATM layer has 4 groups of RxClav/RxEnb* pairs to control 4 PHY groups. All PHYs of one group are connected to the respective RxClav/RxEnb* pair. The RxAddr[3:0] lines are connected to all PHYs. This is shown in the figure below:

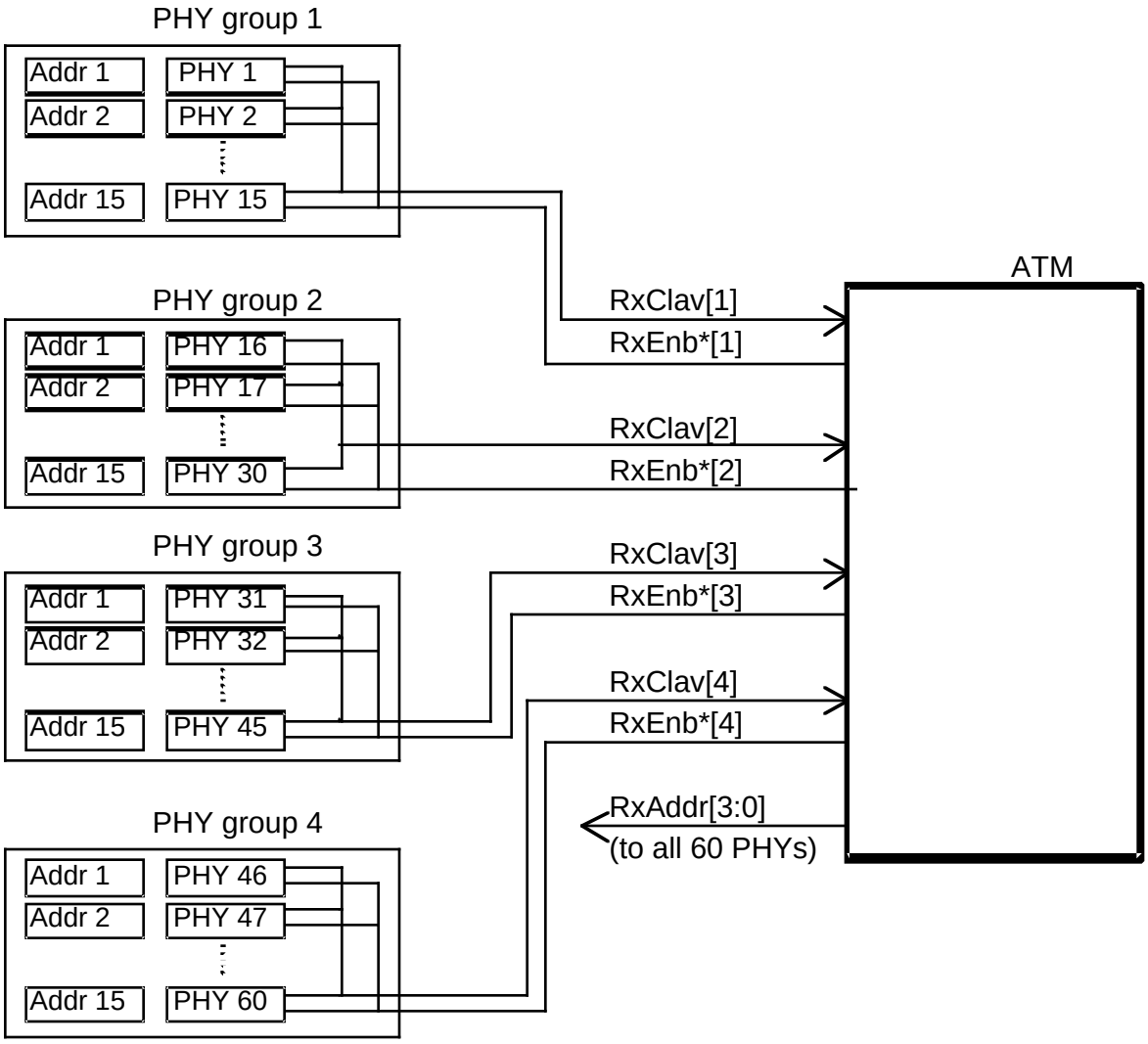


Figure A1.1. Configuration for a System with a Large Number of PHYs

At the Transmit interface TxClav/TxEnb* line pairs are added accordingly.

Up to 15 PHYs can be addressed in each group, resulting in a theoretical limit of 60 PHYs. All 4 PHY groups can be polled in one polling cycle of 30 clock cycles as shown:

cycle 1	get Rx/TxClav information from PHYs	1	16	31	46
cycle 2	get Rx/TxClav information from PHYs	2	17	32	47
...					
cycle 15	get Rx/TxClav information from PHYs	15	30	45	60.

Note that within each group several PHYs could be contained in one package. This has no implications on the addressing. It is assumed that if an integrated multi-PHY contains e.g. 5 PHYs, it has 5 different addresses programmed into the chip.

A1.2 Special cases

A. Each group consists of only one PHY. In this case the address lines RxAddr[3:0] and TxAddr[3:0] can remain unconnected. The ATM controls 4 PHYs, each operating in level 1 mode.
B. Only one PHY group is used. This is the level 2 mode.

A2.3 Impact on the PHY Layer

None

A2.4 Impact on the ATM Layer

The additional RxClav/RxEnb* and TxClav/TxEnb* signal pairs are an optional enhancement. In case of only one PHY group there is no impact on the ATM layer.

Appendix 2. Management Interface

A2.1 Scope

This section is included as an appendix to the Utopia level 2 specification. The management interface(s) is(are) provided as a guideline to implementors. ATM and PHY layers are fully conformant to the Utopia level 2 specification if they implement the main parts of this specification, even if they incorporate a management interface different to those described here within.
This implementation guideline is provided to further extend the scope of interoperability provided by the Utopia level 2 specification.

A2.2 Introduction

According to Utopia level 1 specification (V2.01, March 21, 1994), the management interface of a PHY device is connected to a Management Entity (uP), see Figure A2.1.

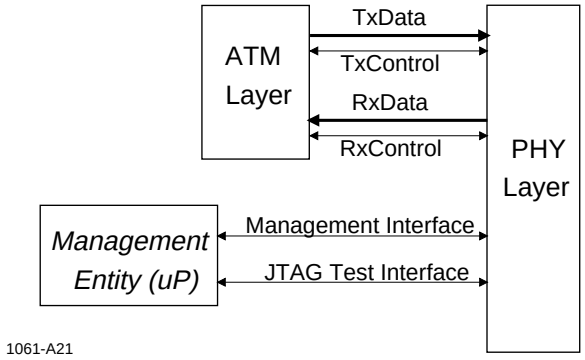


Figure A2.1: Utopia Interface Diagram (Source: Utopia level 1, Figure 1, page 1)

A2.3 Serial interface

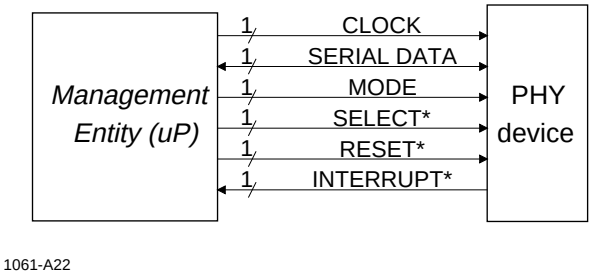


Figure A2.2: Serial management interface according to the Utopia Interface Diagram

A2.3.1 Signals

The following signals are defined as required (**R**) for the serial management interface of a PHY device. Signals and their usage are described in Table A2.1. The terms uP⇒P and uP⇐P (column DIR, Direction) define an unidirectional signal from the microprocessor to the PHY device and vice versa. uP⇔P defines a bi-directional signal between the microprocessor and the PHY device.

Table A2.1: List of interface signals (serial interface)

Signal	DIR	Description
DATA	uP⇔P	Signal DATA carries the bit-serial data, address and two control bits. Any information is read in at the positive (rising) edge of CLOCK. Any information is output with the positive (rising) edge of CLOCK. For writing into the PHY device (control bits, address bits, write data) DATA is only valid if SELECT* is LOW at the same clock edge. For a data byte transfer out of the PHY device, DATA is valid at the next rising clock edge when SELECT* is LOW.
CLOCK	uP⇒P	Free running clock signal.
MODE	uP⇒P	Distinction between an address and control/data transfer. LOW: Control or data transfer HIGH: Address transfer.
SELECT*	uP⇒P	Signal SELECT* selects a PHY device and enables the transfer of address, control and data. LOW: PHY device is selected. HIGH: PHY device is not selected and ignores the signals DATA and MODE. PHY device holds its output driver of DATA in high impedance state (input mode).
RESET*	uP⇒P	LOW: PHY device is forced to reset. The output driver of DATA is set into its high impedance state (input mode). RESET must be LOW at least for one clock cycle. HIGH: PHY device does not reset.
INTR*	uP⇐P	Level sensitive interrupt signal generated by the PHY device. Open-drain active low output. INTR* must be LOW at least for one clock cycle.

SELECT, CLOCK and RESET must be driven HIGH or LOW by the microprocessor at any time. MODE and DATA may float as long as no PHY device is selected (SELECT* is HIGH, microprocessor may hold its output driver of DATA and MODE in high impedance state)

A2.3.2 Operation

A transfer of data (transfer cycle) is initiated by asserting SELECT* to LOW. First, two control bits and (optional) the address information is transferred (written) into the PHY device. Second, data information is transferred (read/write). Thus, a transfer cycle is as follows:

* Asserting SELECT* from HIGH to LOW initiates the transfer cycle. The PHY device detects SELECT* to be LOW at the next rising (positive) clock edge (edge #1). MODE and DATA are don't care (may float) at clock edge #1.
* On the next rising clock edge (edge #2), the signal DATA defines the direction of the following data transfer by control bit C1 (control bit C1 LOW: read cycle, HIGH: write cycle). MODE should be LOW at this clock edge #2 if no new address is transferred in front of the first data transfer, otherwise MODE must be HIGH.
* On the next rising clock edge (edge #3), the signal DATA defines the address increment mode by control bit C2:

- LOW: Automatic address increment mode.
  Multiple read/write byte operations are executed on successive byte locations (starting at a given address), e.g. used to read/write from/to successive configuration registers. The internal address register is automatically incremented after each data byte transfer. The PHY device must define its behavior in case of address wrap around. Read/write transfers from/to byte locations not implemented in the PHY device are dummy cycles.
- HIGH: Single address mode.
  Multiple read/write operations are executed at the same address (e.g. read/write from/to a FIFO port).

In any case, control bits C1 and C2 must be transferred. For a single data byte transfer, both address modes can be applied.
At this considered clock edge #3, the PHY device may preset (preload) its internal address register to a predefined value (reload the address register with a new (fix or programmable) value). Otherwise the address register stays unchanged. Conditions for preloading is up to individual PHY device designs. This is independent whether the microprocessor writes address information in front of the first data transfer or not.
If MODE is LOW at clock edge #2 or clock edge #3, no new address is written into the PHY device in front of the first data transfer. Data byte transfer starts after one additional clock cycle as described below.
If MODE is HIGH at clock edge #2 and clock edge #3, the most significant bit of a new address is read in at the next rising clock edge (edge #4) by the PHY. In general, MODE must be HIGH for two clock cycles prior to any first transferred (most significant) address bit.

* Remaining address information is read in by the PHY device on the following rising clock edges as long as MODE is HIGH. The number of address bits written into the PHY device may be less then the size of the internal address register. The new received address information overwrites (least significant bit adjusted) the correspondent part of the address register. The number of address bits written into the PHY device may be more then the size of the internal address register. Only the least recently received address information overwrites (least significant bit adjusted) the address register.
* For read and write transfers, the output of data is started one clock cycle after MODE is detected to be LOW (there is always a one clock cycle gap between the last received address bit and the first (read/write) data bit). Then data bits are output and read in on every following rising clock edge. Data bytes are read/written in units of 8 data bits (most significant data bit first). Multiple data byte transfers are executed as long as SELECT* is LOW.
* SELECT* should stay LOW at least for one data byte transfer. SELECT* must go HIGH only on a data byte boundary to end a transfer. Reading/writing the least significant bit D0 of a data byte and detecting SELECT* to be HIGH terminates the transfer. If SELECT* is deasserted to HIGH not on a data byte boundary, the current transfer must be aborted immediately. Only data bytes which have been completely read/written from/to the PHY device are valid.
* SELECT* must be HIGH between two transfer cycles at least for one clock cycle.
* During a transfer cycle, a new address can be written into the PHY device in front of each data byte transfer. In case the PHY device reads/writes the least significant bit D0 of a data byte and detects MODE to be HIGH, the transfer of a new address into the PHY device is started after one additional clock cycle (note, MODE must be HIGH for two clock cycles prior to the first transferred address bit). After the address transfer, data byte transfer is resumed as described above.

A2.3.3 Examples

In the following examples, it is assumed that a microprocessor reads/writes from/into a PHY device. All examples start with no data transfer being active.

A2.3.3.1 Read Operation

Figure A2.3 shows an example of a single data byte read transfer, the transfer of three address bits and the preloading of the internal address register. The individual rising clock edges are numbered from 1 to 16. The following Table A2.3 describes the actions at these rising clock edges. The internal address register holds 55h (01010101b) from a previous transfer cycle. Furthermore, this examples shows MODE be either tri-stated or don't care if no PHY device is selected.

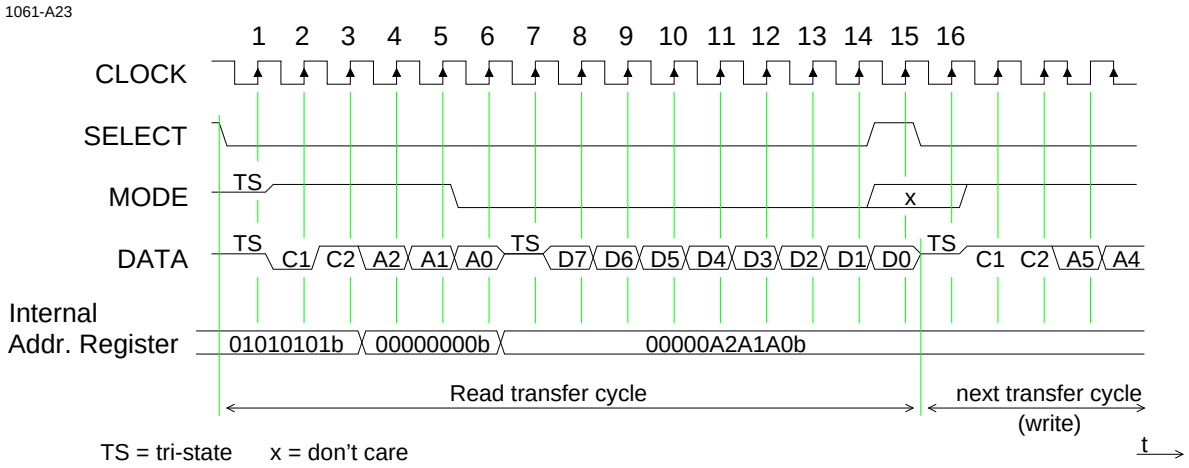


Figure A2.3: Single data byte read transfer

Table A2.3: Single data byte read transfer

Clock #	Description
1	The PHY device detects SELECT* to be LOW. It awaits the first control bit C1 at (next) rising clock edge #2. MODE and DATA are don't care at this clock edge. The Microprocessor outputs the first control bit (C1) and MODE with this rising clock edge.
2	The PHY device reads control bit C1. It is LOW, thus read cycle. The Micropro-cessor outputs the second control bit (C2) with this rising clock edge.
3	The PHY device reads in control bit C2. It is HIGH, thus single address mode. MODE is HIGH for two clock cycles, thus PHY device awaits first address bit at (next) rising clock edge #4. In this example, the internal address register is preloaded with 00000000b (00h) with this rising clock edge.
4,5,6	The PHY device reads in address bits A2, A1, A0.
6	The PHY device detects MODE to be LOW. Thus (next) rising clock edge #7 is not used and The PHY device will output the first data bit with rising clock edge #7, valid for the microprocessor at clock edge #8. The microprocessor must switch its output driver of DATA into high impedance state (input mode) with this rising clock edge #6. The received address bits A2, A1, A0 overwrite the three least significant bits of the address register. The internal address register now holds the new address 00000A2A1A0b.
7	The PHY device outputs data bit D7 with this rising clock edge (MSB first).
8	The microprocessor reads in data bit D7 at this clock edge. The PHY device outputs data bit D6 with this rising clock edge.
9, 10, 11 12, 13, 14	The microprocessor reads in data bits D6 to D1 at these clock edges. The PHY device outputs data bits D5 to D0 with these rising clock edges.
14	The microprocessor reads only one data byte, thus it deasserts SELECT* to HIGH with this clock edge.
15	The microprocessor reads in the data bit D0. The PHY device detects SELECT* to be HIGH. Thus, the PHY device ends transfer at this clock edge and switches its DATA output driver into a high impedance state (input mode).

Figure A2.4 shows an example of a multiple data bytes read transfer. The internal address register holds 3Ah from a previous transfer cycle. Control bit C2 is LOW, thus data bytes are read from successive byte locations inside the PHY device. Note, the end of the transfer is controlled by the microprocessor only by the signal SELECT. In this example, with rising clock edge #3, the internal address register is preloaded with 20h. Three address bits are written into the PHY device (A2,A1,A0 = 101b, 05h). Thus, with rising clock edge #6 the address register holds 25h. To address the successive bye locations, the internal address register is incremented (in this example) one clock cycle prior to the next data transfer.

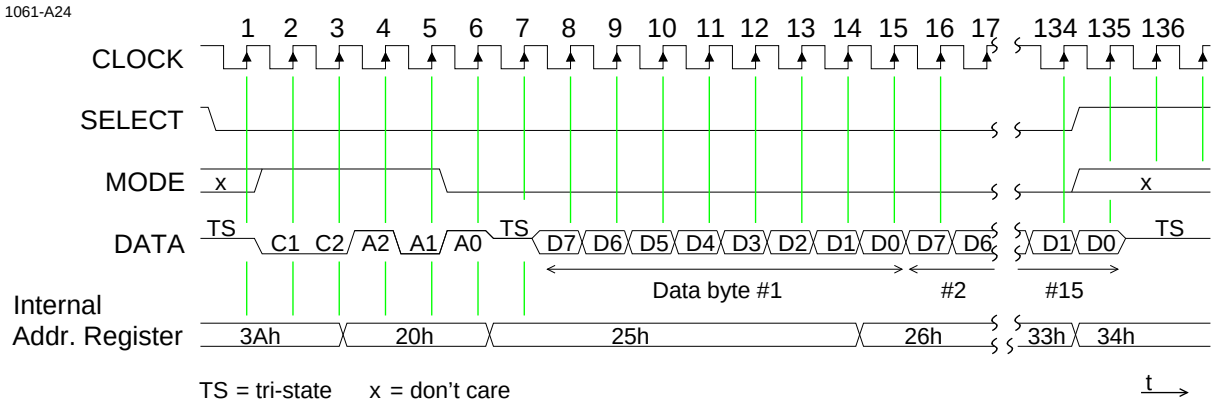


Figure A2.4: Multiple data byte read transfers (successive byte locations)

A2.3.4 Write Operation

Figure A2.5 shows an example of a multiple data bytes write transfer, aborted by the microprocessor during the transfer of the second data byte. New address information is written into the PHY device between the first and the second data byte. The individual positive clock edges are numbered from 1 to 20. Table A2.3 describes the actions at these clock edges. The internal address register holds 41h from a previous transfer cycle. Control bit C2 is LOW, thus data bytes are written into successive byte locations inside the PHY device.

Note: Read and write transfer cycle timings are in principle the same. Except that phases marked x (don't care, DATA, Figure A2.5) in the write cycle are tri-stated in the read cycle. In the read cycle, this allows the switch over of the low impedance driver side from the microprocessor to the PHY device and vice versa.

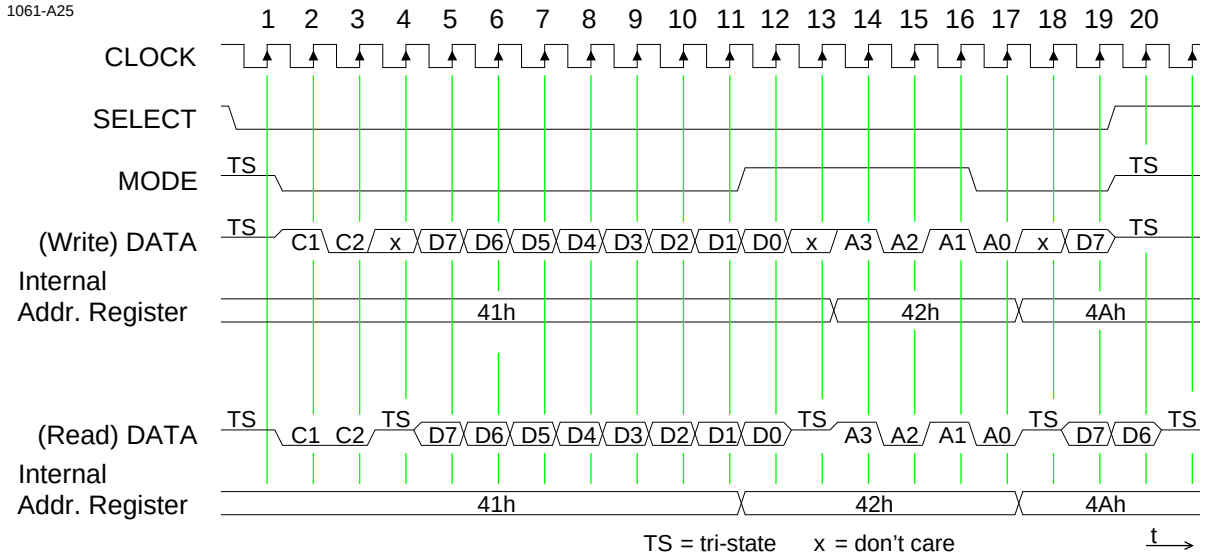


Figure A2.5: Multiple data byte write (read) transfer (aborted)

Table A2.3: Single data byte write transfer (part 1 of 2)

Clock #	Description
1	The PHY device detects SELECT* to be LOW. It awaits the first control bit C1 at (next) rising clock edge #2. MODE and DATA are don't care at this clock edge. The microprocessor outputs the first control bit (C1) and MODE with this rising clock edge.
2	The PHY device reads control bit C1. It is HIGH, thus write cycle. The micropro-cessor outputs the second control bit (C2) with this rising clock edge. MODE is LOW, thus no address in front of first data transfer.
3	The PHY device reads control bit C2. It is LOW, thus automatic address increment mode. MODE is LOW, thus no address in front of first data transfer. In this example, no preload of the internal address register at this clock edge. The microprocessor may output first data bit (MSB, D7) already with this rising clock edge.
4	Not used, DATA is don't care. The microprocessor must output first data bit (MSB, D7) latest with this rising clock edge.
5	The PHY device reads in data bit D7. The microprocessor outputs data bit D6 with this rising edge.
6,7,8,9, 10, 11	The PHY device reads in data bits D6 to D1 at these clock edges. The micropro-cessor outputs data bits D5 to D0 on these edges. With rising clock edge #11, MODE is set HIGH by the microprocessor, indicating an address transfer after this data byte transfer (detected by the PHY device at clock edge #12).
11	With rising clock edge #11, the PHY device increments the internal address register to be prepared for the next byte transfer (control bit C2 was LOW: automatic address increment mode for this transfer cycle).
12	The PHY device reads in data bit D0. The PHY device detects MODE to be HIGH. Thus, the PHY device prepares itself for an address transfer (it reads in new address starting with rising clock edge #14). The microprocessor may output the most significant address bit (in this example: A3) already with this rising clock edge.
13	DATA is don't care. The microprocessor must output most significant address bit (in this example: A3) latest with this rising clock edge.
13	PHY device: data is written in the into byte location at address 41h. To address the successive byte locations, the internal address register is incremented (in this example) one clock cycle after a complete data transfer.
14,15,16 17	The PHY device reads address bits A3, A2, A1, A0.
17	PHY device: received address bits A3, A2, A1, A0 overwrite the four least significant bits of the address register. Thus, the internal address register now holds new address 4Ah.
17	The microprocessor may output first data bit (D7, MSB) already with this rising clock edge.
18	Not used, DATA is don't care. The microprocessor must output first data bit (D7, MSB) latest with this rising clock edge.

Table A2.3: Single data byte write transfer (part 2 of 2)

Clock #	Description
19	The PHY device reads in data bit D7. The microprocessor aborts transfer cycle by deasserting SELECT* to HIGH with this rising clock edge. Thus, it outputs don't care instead of data bit D6 with this rising edge.
20	The PHY device detects SELECT* to be HIGH and aborts transfer too. No data is written into byte location 4Ah.

A2.3.5 A.C. characteristics

The A.C. characteristics for the serial management interface are based on the timing specification for the receiver side of a signal, see Figure A2.6. This is analogous to chapter 5.1 of this document. The setup and the hold times are defined with regard to a rising (positive) clock edge. Taking the actual used clock frequency into account (e.g. up to the max. frequency), the corresponding (min. and max.) transmit side "clock to output" propagation delay specifications can be derived. The timing references (tT5 to tT12) are according to tables A2.4 to A2.6.
The notes in the following chapters A2.3.5.1 to A2.3.5.3 refer to appendix A2.5 of this document. The common conditions for the A.C. characteristics of the serial interface are described in chapter 5.1.9 of this document.

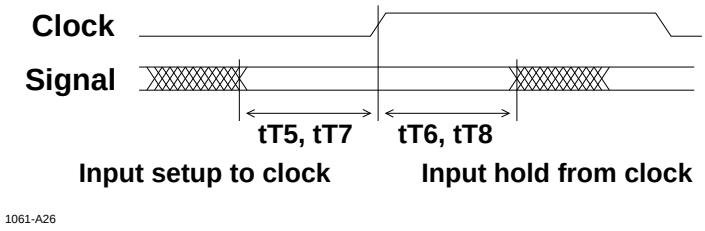


Figure A2.6: Setup and hold time definition (serial management interface)

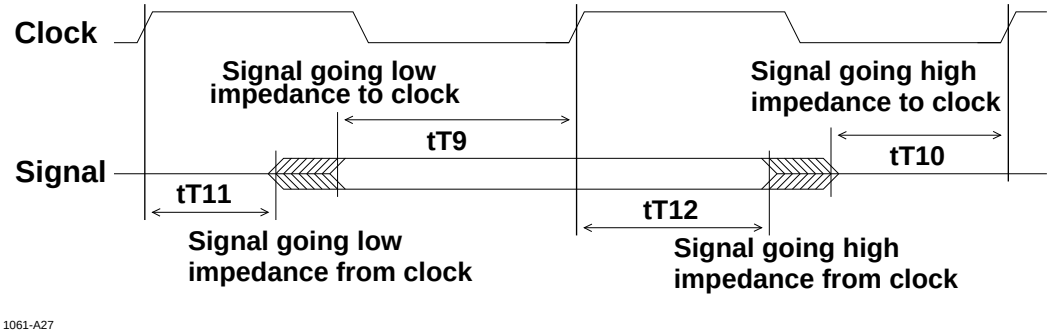


Figure A2.7: Tri-state timing definition (serial management interface)

A2.3.5.1 25 MHz interface

Table A2.4: 25 MHz timing (serial interface)

Signal	DIR	Item	Description	Min.	Max.
CLOCK	uP⇒P	f1	TxClk frequency (nominal)	0	25 MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	4ns
MODE, SELECT*, RESET*	uP⇒P	tT5	Input setup to CLOCK	10ns	-
		tT6	Input hold from CLOCK	1ns	-
INTR*	uP⇐P	tT7	Input setup to CLOCK	10ns	-
		tT8	Input hold from CLOCK	1ns	-
DATA	uP⇔P	tT9	Signal going low impedance to CLOCK	10ns	-
		tT10	Signal going high impedance to CLOCK(1)	0ns	-
		tT11	Signal going low impedance from CLOCK	1ns	-
		tT12	Signal going high impedance from CLOCK	1ns	-

A2.3.5.2 33 MHz interface

Table A2.5: 33 MHz timing (serial interface)

Signal	DIR	Item	Description	Min.	Max.
CLOCK	uP⇒P	f1	TxClk frequency (nominal)	0	33 MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	3ns
MODE, SELECT*, RESET*	uP⇒P	tT5	Input setup to CLOCK	8ns	-
		tT6	Input hold from CLOCK	1ns	-
INTR*	uP⇐P	tT7	Input setup to CLOCK	8ns	-
		tT8	Input hold from CLOCK	1ns	-
DATA	uP⇔P	tT9	Signal going low impedance to CLOCK	8ns	-
		tT10	Signal going high impedance to CLOCK(1)	0ns	-
		tT11	Signal going low impedance from CLOCK	1ns	-
		tT12	Signal going high impedance from CLOCK	1ns	-

A2.3.5.3 50 MHz interface

Table A2.6: 50 MHz timing (serial interface)

Signal	DIR	Item	Description	Min.	Max.
CLOCK	uP⇒P	f1	TxClk frequency (nominal)	0	50 MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	2ns
MODE, SELECT*, RESET*	uP⇒P	tT5	Input setup to CLOCK	4ns	-
		tT6	Input hold from CLOCK	1ns	-
INTR*	uP⇐P	tT7	Input setup to CLOCK	4ns	-
		tT8	Input hold from CLOCK	1ns	-
DATA	uP⇔P	tT9	Signal going low impedance to CLOCK	4ns	-
		tT10	Signal going high impedance to CLOCK(1)	0ns	-
		tT11	Signal going low impedance from CLOCK	1ns	-
		tT12	Signal going high impedance from CLOCK	1ns	-

A2.4 Parallel interface

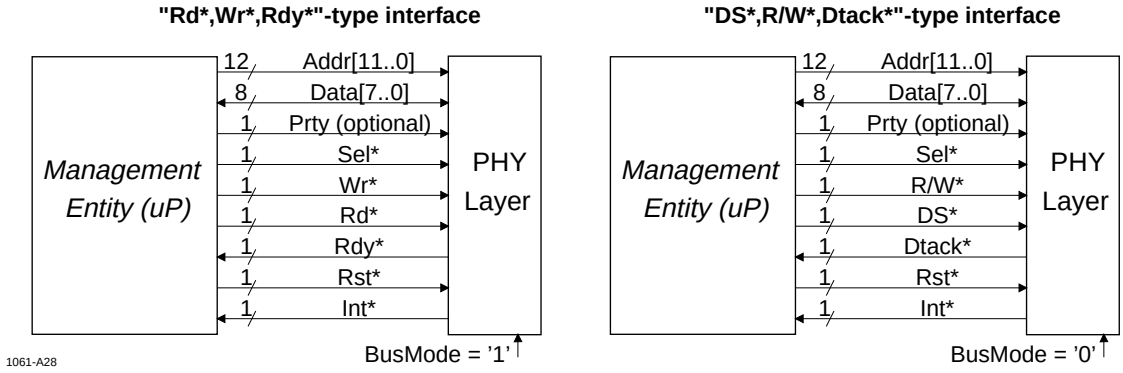


Figure A2.8: Parallel management interface according to the Utopia Interface Diagram

A2.4.1 Signals

Table A2.7: List of optional interface signals (parallel interface)

Signal	DIR	Description
Prty	uP⇔P	Prty is optional (**O**) bidirectional odd Data parity.

Table A2.8: List of required interface signals (parallel interface)

Signal	DIR	Description
BusMode	uP⇒P uP⇒A	Input to ATM and PHY to select the mode of operation of the management interface. BusMode = '1' provides a <Rd*;Wr*;Rdy*> style (Intel compatible) interface; and BusMode = '0' provides a <DS*;R/W*;Dtack*> style (e.g. Motorola 68K, Intel i960 compatible) interface.
Addr[11..0]	uP⇒P	MSB is Addr[11]. The upper 64 bytes are reserved for up to 32 address pointers to registers describing each of the attached PHY devices.
Data[7..0]	uP⇔P	Byte-wide bidirectional data bus. MSB is Data[7].
Sel*	uP⇒P	Select. Active low enable signal used to validate the Addr bus for read and write transfers.
Rd* or DS*	uP⇒P	Read, or Data Strobe. If BusMode = '1', the active low Rd* input is LOW to enable read data from the addressed location onto the Data bus. If BusMode = '0' the active low DS* input is LOW to enable read data from the PHY layer, or strobe write data into the PHY layer.
Wr* or R/W*	uP⇒P	Write, or Read/Write. If BusMode = '1', the active low Wr* input is LOW to write data from the Data bus into the addressed location. If BusMode = '0', this input defines the access as a read if '1' or a write if '0'.
Rdy* or Dtack*	uP⇐P	Ready or Data Acknowledge. Tri-state acknowledge signal LOW to end data transfers over the Data bus. For either BusMode, Rdy*/Dtack* is LOW to complete a transfer.
Rst*	uP⇒P	Reset. Active low (level sensitive) input LOW to reset the PHY layer.
Int*	uP⇐P	Interrupt. Level sensitive interrupt signal LOW by the PHY layer. For either BusMode, Int* is an open-drain active low output.

For the parallel management interface of a PHY device, the signals in Table A2.8 are defined as required (**R**), the signals in Table A2.7 are defined as optional (**O**).

In Tables A2.7 and A2.8 the terms uP⇒P and uP⇐P (column DIR, Direction) define an unidirectional signal from the microprocessor to the PHY layer and vice versa. uP⇔P defines a bi-directional signal between the microprocessor and the PHY layer (the same applies for the ATM layer, uP⇒A).

A2.4.2 Operation

A2.4.2.1 Overview

This interface is designed to support most microprocessors. A BusMode pin selects one of two timing interfaces, Intel-compatible or Motorola-compatible. A ready/data_ack control is provided to support asynchronous or synchronous transfer cycles.
There are 3 control lines for effecting transfers. BusMode = '0' provides a read/write selector, a data strobe and a data acknowledge. BusMode = '1' provides a read strobe, a write strobe and a ready acknowledgment. The following text uses BusMode = '1' signal names, with BusMode = '0' names in parentheses.

A2.4.2.2 Timing

For the parallel interface, the common conditions for the A.C. characteristics are described in chapter 5.1.9 of this document.

A2.4.2.2.1 Write Cycles

The ATM layer performs write cycles by driving the address onto **Addr**, driving **Data** with the byte to be written, and asserting the appropriate strobes. The PHY layer will drive **Rdy*** (**Dtack*)** valid within the specified time, and assert **Rdy*** (**Dtack*)** to signal completion of the transfer. The PHY layer must tri-state **Rdy*** (**Dtack***) and **Data** whenever it is not selected. For BusMode = '1' the data is strobed by asserting the **Wr*** signal, with **Rd*** HIGH. For BusMode = '0' the data is strobed by asserting **DS*** and setting **R/W*** to a '0'. The following PHY device timings in table A2.9 apply to Figure A2.9.

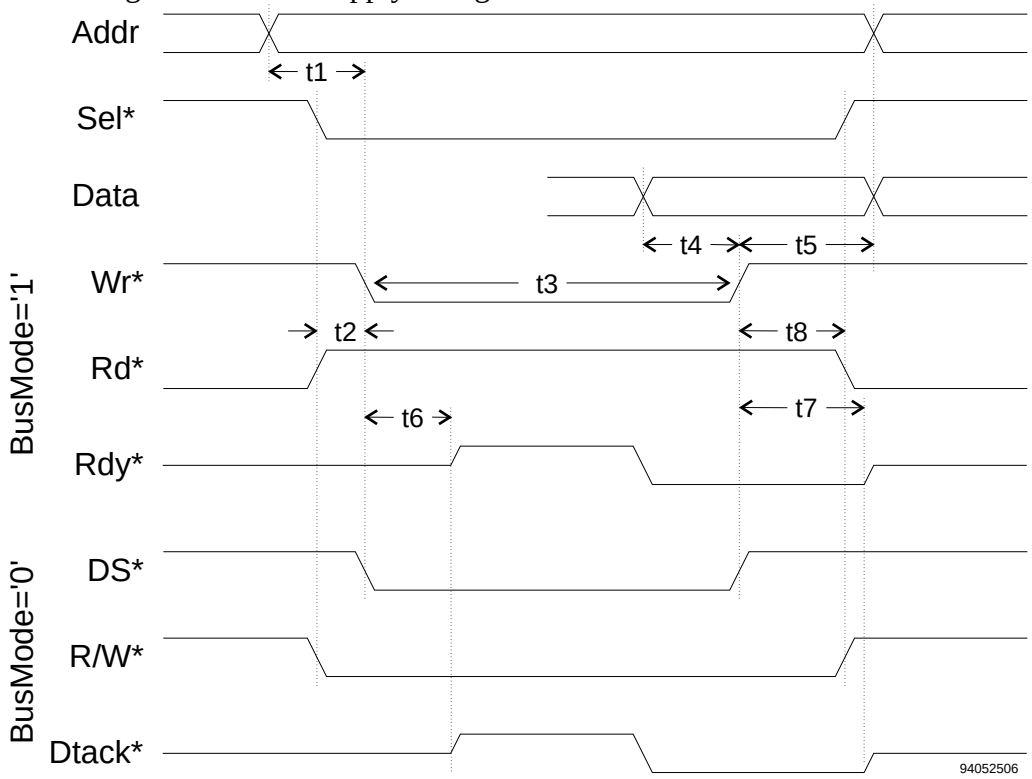


Figure A2.9: Single data byte write transfer (parallel interface)

Table A2.9: Transmit timing (parallel interface)

Item	Description	Min.	Max.
t1	Addr setup to Wr* (DS*) assertion	10 ns	
t2	Sel* (Sel*, R/W*) setup to Wr* (DS*) assertion	5 ns	
t3	Wr* (DS*) pulse width	50 ns	
t4	Data setup to Wr* (DS*) deassertion	15 ns	
t5	Addr, Data hold from Wr* (DS*) deassertion	4 ns	
t6	Rdy* (Dtack*) valid from Wr* (DS*) assertion		15 ns
t7	Rdy* (Dtack*) tri-state from Wr* (DS*) deassertion		10 ns
t8	Sel* (Sel*, R/W*) hold from Wr* (DS*) deassertion	0 ns	

A2.4.3 Read Cycles

The ATM layer performs read cycles by driving the address onto **Addr**, and asserting **Sel*** and the appropriate strobes. The PHY layer will drive **Rdy* (Dtack*)** valid within the specified time, drive **Data** with the requested byte, and assert **Rdy* (Dtack*)** to signal completion of the transfer. The PHY layer must tri-state **Rdy* (Dtack*)** and **Data** whenever it is not selected. For BusMode = '1' the data is strobed by asserting the **Rd*** signal, with **Wr*** HIGH. For BusMode = '0' the data is strobed by asserting **DS*** and setting **R/W*** to a '1'. The following PHY device timings in table A2.10 apply to Figure A2.10.

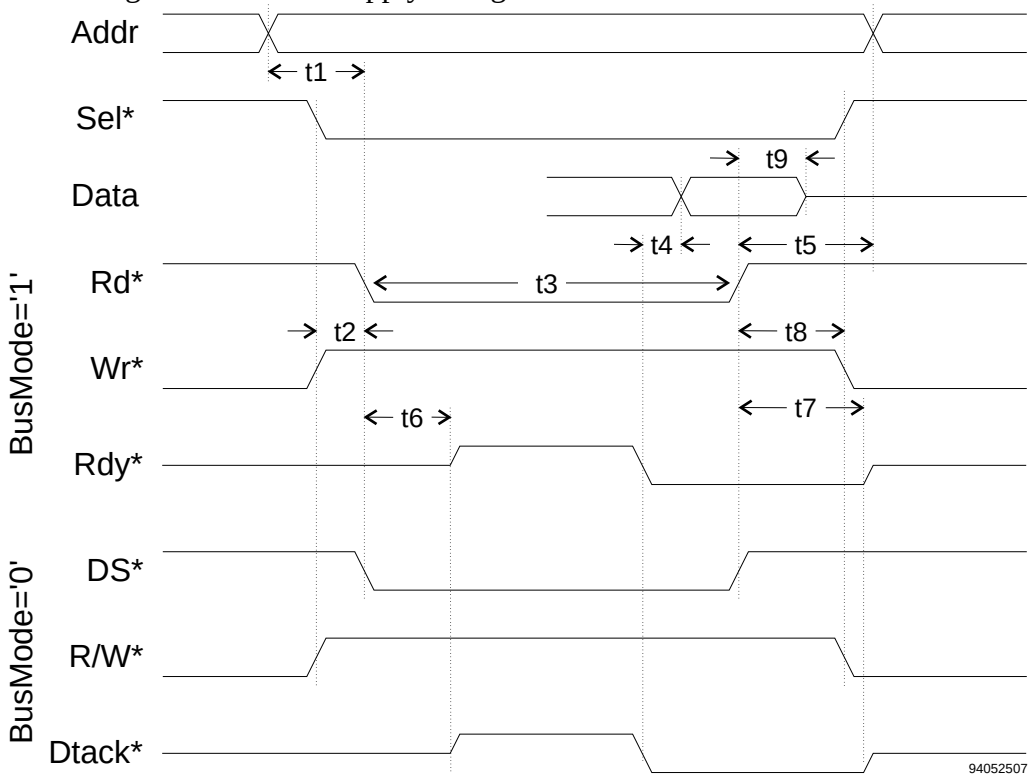


Figure A2.10: Single data byte read transfer (parallel interface)

Table A2.10: Receive timing (parallel interface)

Item	Description	Min.	Max.
t1	Addr setup to Rd* (DS*) assertion	10 ns	
t2	Sel* (Sel*, R/W*) setup to Rd* (DS*) assertion	5 ns	
t3	Rd* (DS*) pulse width	50 ns	
t4	Data valid from Rdy* (Dtack*) assertion		10 ns
t5	Addr hold from Rd* (DS*) deassertion	4 ns	
t6	Rdy* (Dtack*) valid from Rd* (DS*) assertion		15 ns
t7	Rdy* (Dtack*) tri-state from Rd* (DS*) deassertion	10 ns	
t8	Sel* (Sel*, R/W*) hold from Rd* (DS*) deassertion	0 ns	
t9	Data invalid/tri-state from Rd* (DS*) deassertion	15 ns	

A2.5 D.C. characteristics

The following chapters A2.5.1 and A2.5.2 list the D.C. characteristics for the serial and parallel management interface. The parameters assume, that the PHY device and management entity (microprocessor) are located close to each other, minimizing transmission line effects.

A2.5.1 Serial interface

Table A2.11: D.C. characteristics (serial interface)

Symbol	Parameter	Min.	Max.	Conditions
VIL	Input LOW voltage	-0,3V	+0.8V	(3)
VIH	Input HIGH voltage	+2.0V	VDD + 0.3V	(4)
VOH	Output or bi-directional HIGH voltage	+2.4V	-	IOH ≥ |-4mA| (5)
VOL	Output or bi-directional LOW voltage	-	+0,5V	IOL ≥ +4mA (6)
IOH	Output current at HIGH voltage	-4mA	-	VOH ≥ +2.4V (7)
IOL	Output current at LOW voltage	+4mA	-	VOL ≤ +0.5V (8)
IIH	Input current at HIGH voltage	-	-	(9)
IIL	Input current at LOW voltage	-	-	(9)

A2.5.2 Parallel interface

Table A2.12: D.C. characteristics (parallel interface)

Symbol	Parameter	Min.	Max.	Conditions
VIL	Input LOW voltage	-0,3V	+0.8V	(3)
VIH	Input HIGH voltage	+2.0V	VDD + 0.3V	(4)
VOH	Output or bi-directional HIGH voltage	+2.4V	-	IOH ≥ |-8mA| (10)
VOL	Output or bi-directional LOW voltage	-	+0,5V	IOL ≥ +8mA (11)
IOH	Output current at HIGH voltage	-8mA	-	VOH ≥ +2.4V (12)
IOL	Output current at LOW voltage	+8mA	-	VOL ≤ +0.5V (13)
IIH	Input current at HIGH voltage	-	-	(9)
IIL	Input current at LOW voltage	-	-	(9)

A2.5.3 Common D.C. characteristics

Table A2.13: Common parameters for D.C. characteristics

Parameter	Typ.	Min.	Max.
Temperature range (Tambient) (14)	-	0 to +70ßC	-
Power supply VDD (2)	+5V or +3,3V	-	-
Power supply Tolerance (15)	-	Ò5%	-

A2.6 Notes

(1) This gives one clock period time for the active driver to switch in the high impedance state (signal going high impedance 0ns *in front of next* CLOCK).

(2) This specification defines either VDD = +5V or VDD = +3,3V. It assumes the same VDD on the transmit and receive side of a signal. It does not consider a mixed VDD (+5V/+3,3V) configuration.

(3) A PHY device with VIL, min. ≤ -0.3V is compliant to this specification.

(4) A PHY device with VIH, max. ≥ VDD+0.3V is compliant to this specification.

(5) Negative current flows out of the considered node (out of the PHY device pin). A PHY device with VOH, min. ≥ +2.4V (and IOH ≥ |-4mA|) is compliant to this specification.

(6) Positive current flows into the considered node (into the PHY device pin). A PHY device with VOL, max. ≤ +0.5V (and IOL ≥ +4mA) is compliant to this specification.

(7) Negative current flows out of the considered node (out of the PHY device pin). IOH, min. defines the minimal required IOH value for the driver.

A PHY device with IOH, min. ≥ |-4mA| (and VOH ≥ +2.4V) is compliant to this specification.

(8) Positive current flows into the considered node (into the PHY device pin). IOL, min. defines the minimal required IOL value for the driver.

A PHY device with IOL, min. ≥ +4mA (and VOL ≤ +0,5V) is compliant to this specification.

(9) To allow several technologies, no values for IIH and IIL are specified. An input can sink and source.

(10) Negative current flows out of the considered node (out of the PHY device pin). A PHY device with VOH, min. ≥ +2.4V (and IOH ≥ |-8mA|) is compliant to this specification.

(11) Positive current flows into the considered node (into the PHY device pin). A PHY device with VOL, max. ≤ +0.5V (and IOL ≥ +8mA) is compliant to this specification.

(12) Negative current flows out of the considered node (out of the PHY device pin). IOH, min. defines the minimal required IOH value for the driver.

A PHY device with IOH, min. ≥ |-8mA| (and VOH ≥ +2.4V) is compliant to this specification.

(13) Positive current flows into the considered node (into the PHY device pin). IOL, min. defines the minimal required IOL value for the driver.

A PHY device with IOL, min. ≥ +8mA (and VOL ≤ +0,5V) is compliant to this specification.

(14) A PHY device with a temperature rangeof at least 0 to +70ßC is compliant to this specification.

(15) A PHY device with a power supply voltage tolerance ≥ 5% is compliant to this specification.

Appendix 3. References

[1] The ATM Forum, “Utopia, An ATM-PHY Interface Specification, Level 1, Version 2.01”, March 21, 1994

[2] Garg et al, “The ATM Forum Contribution 94-850 and 850 R1”, Utopia, Level 1, Versions 0.1, and 0.5”, July and September 1994.