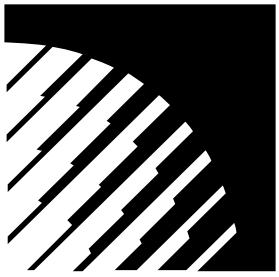

The ATM Forum Technical Committee

UTOPIA 3 Physical Layer Interface

af-phy-0136.000

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1. Introduction

1.1 Document Purpose and Background

This document describes a new generation of *the Universal Test & Operations PHY Interface for ATM (UTOPIA)* data path interfaces. The Utopia Level 3 specification provides similar functionality as the Utopia Level 1 & 2 interfaces [1], [2] but will cater for higher data rates. Familiarity with the Level 1 and Level 2 Utopia documents would be beneficial to the reader but is not required.

The Level 1 and Level 2 Utopia specifications describe the data path between a Physical layer device and an ATM layer device, utilizing a 8-bit or 16-bit data path, catering for data rates of up to 800 Mb/s. The control of the data exchange is performed using cell-level handshaking.

Whilst this Utopia Level 3 specification will build on concepts described in [1] and [2], a large number of changes and improvements have been made and this document can be used on its own.

1.2 Scope

The Utopia Level 3 specification has been generated to match the development in Physical layer interface standards towards higher interface rates (1.2 Gb/s, 2.4 Gb/s). The data path described in this specification allows for data transport at rates of up to 3.2 Gb/s.

1.2.1 Definition of AC and DC Characteristics

The description of AC characteristics features the nominal bus bandwidth and the clocking scheme:

1) 32-bit, 16-bit or 8-bit data path

2) The nominal bus bandwidth of 3.2 Gb/s (32-bit mode), 1.6 Gb/s (16-bit mode) or 800 Mb/s (8-bit mode)

3) Single-edged clocking of data and control/status signals

The description of DC characteristics features the target voltage level:

Vdd = 3.3V nominal. The voltage levels of the signals described in this specification are referenced to Vdd, as shown in section 5.2.

1.3 Statement of Compatibility with Level 2 Document

The Utopia Level 3 interface as specified in this document is **NOT** backwards compatible with the Level 1 and Level 2 interfaces. Both data bus width and handshaking mechanisms have changed, making direct interfacing between a Utopia Level 3 interface and a Level 1 or 2 interface not possible.

1.4 Document Contents

1) This document describes the Utopia Level 3 interface in terms of functionality.

2) Additional signal definitions.

3) Modified interface handshaking.

4) Detailed AC and DC characteristics.

2. Functional Description

2.1 Conventions

The conventions used in this document are the same as those used in the previous Utopia specifications and are included below for completeness.

The signal direction naming used in this specification is *Transmit* for ATM to PHY layer transfer and *Receive* for PHY to ATM layer.

All signals are active high, unless denoted via a trailing "*" after the signal name, e.g.

SIGNAL_1 Active High

SIGNAL_2* Active Low

2.2 Terminology related to Utopia Scope

2.2.1 Interface speed

The interface speed will be increased with respect to previous Utopia specifications in order to satisfy the bandwidth requirements. The actual required speed depends on Utopia cell size. Timing parameters are specified at 104 MHz.

2.2.2 Data Path

A 32-bit data path is introduced and is intended for up to 3.2 Gb/s operation. The 16-bit data path is intended for operation of up to 1.6 Gb/s. The 8-bit data path is intended for operation of up to 800 Mb/s.

2.2.3 Physical topology

The physical topology of the Utopia Level 3 interface is as a point-to-point connection. The implementation of this topology uses either a single 32-bit data path, a single 16-bit data path or a single 8-bit data path connecting a single ATM layer device with a single PHY layer device.

2.2.4 MPHY operation

This defines the operation of the interface with multiple PHY ports. This specification only provides for MPHY operation when these ports are implemented in a single Multi-port PHY device.

2.2.5 Cell Transfer Burst mode

Once the transport of a cell has started, a complete cell will be transmitted across the Utopia Level 3 interface. It is not possible to stall the transfer of a cell and all octets/words will have to be transferred consecutively.

2.3 Other Terminology

2.3.1 MPHY Device

A Physical layer device that supports the MPHY interface on Utopia. A MPHY device consists of multiple channels connected through a single Utopia interface.

2.3.2 Multi-port PHY device

A Physical layer device that contains two or more Physical layer interface ports. Such a device would benefit from using the MPHY interface configuration.

2.3.3 PHY Port

A Physical layer port always has a one-to-one correspondence with one Physical Media Dependent (PMD) entity.

2.4 Reference Model and Configurations

2.4.1 Capabilities

The Utopia Level 3 Interface is capable of full-duplex bi-directional transmission of ATM cells between an ATM layer device (ATM) and a Physical layer device (PHY).

2.4.2 Connection Topology

The basic reference model for the Utopia interface is given in Figure 2.1. This shows the information streams between the ATM layer device and the Physical layer device. Transmit data flows from ATM to PHY and Receive data flows from PHY to ATM. Both data streams have control for handshaking.

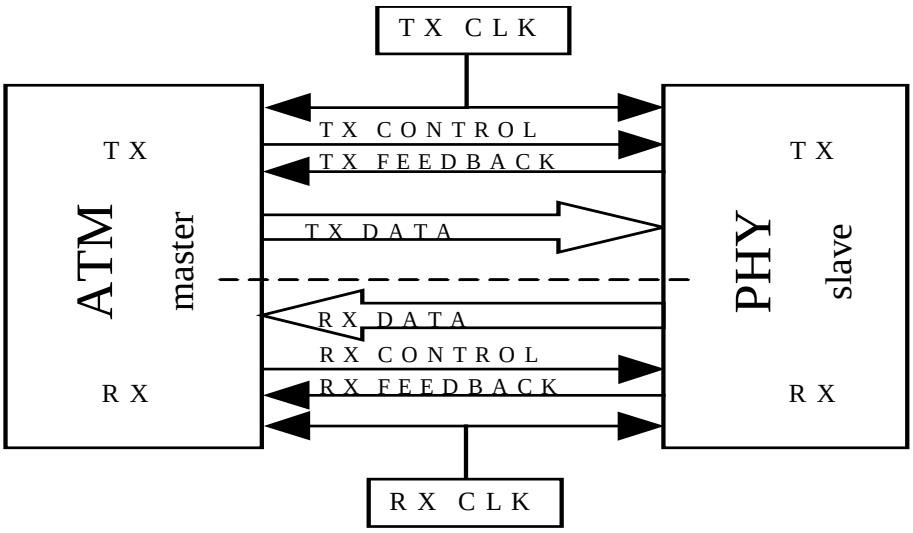


Figure 2.1: Flow of information

A multitude of connection topologies can be required between ATM and PHY devices. The configuration chosen depends on the application in general and the number of ATM and PHY ports to be connected in specific. Figure 2.2 shows the different reference configurations.

This Utopia Level 3 specification covers only the physical connection of a single ATM interface with a single PHY interface. The PHY interface can contain one or more PHY ports, resulting in a connection between the ATM layer device and one or more PHY ports, across a single electrical interface. This means that the electrical connection over the Utopia Level 3 interface will always be point-to-point.

Single 8-, 16- or 32-bit interface

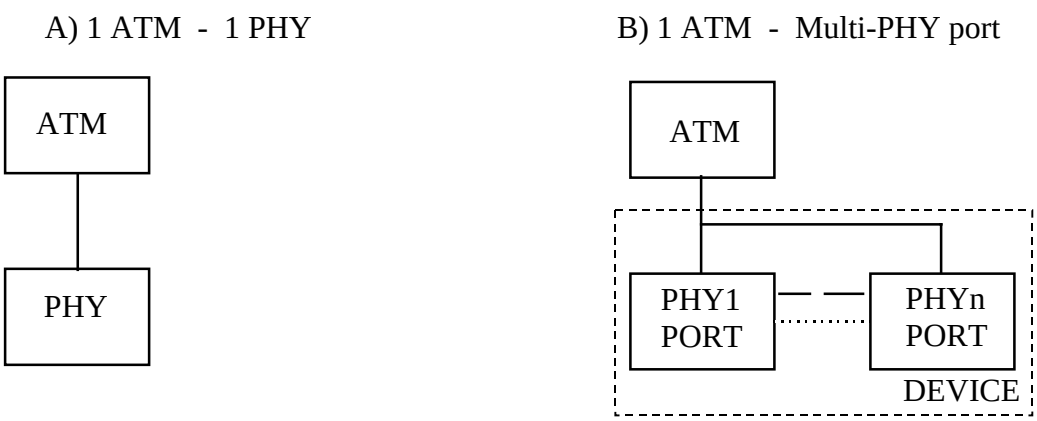


Figure 2.2: Reference Configurations

2.5 Interface Rates

Support of a single 8-bit, 16-bit or 32-bit wide data path in each direction. The 32-bit wide data path shall support the aggregate bandwidth required for an OC-48 line interface. The 16-bit data path shall support the bandwidth for a Gigabit line interface. The 8-bit data path shall support the bandwidth for an OC-12 line interface.

In order to claim compliance with the Utopia Level 3 specification it is required (**R**) to support at least one of the following: the 32-bit wide data path, the 16-bit wide data path or the 8-bit data path as described in this document. Support for multiple data paths is optional (**O**).

2.6 Device Capabilities

The Utopia Level 3 interface specifies a 8-bit, 16-bit or 32-bit data path operating at frequencies of up to 104 MHz. The format of the information transferred across this interface is defined as 52- or 56-octet cells for the 32-bit data path, 52- or 54-octet cells for the 16-bit data path and 52- or 53-octets for the 8-bit data path.

2.7 Cell Processing

2.7.1 32-bit data path

With the introduction of a 32-bit data path, a new cell format is required as the cell size now has to be a multiple of 4 octets. The transfer of 52-octet cells as well as longer cells is allowed.

Only the 52- and 56-octet cell formats are defined in this specification and are as shown in Table 2.1 & Table 2.2. Support for the 52-octet cell format is required (**R**). Support for the 56-octet cell format is optional (**O**). Note that in the 52-octet format there is no field for the transport of the HEC octet. However, transport of the HEC is not required, as this is a part of Physical layer functionality. When transferring the HEC in the 56-octet cell format the HEC shall be transferred in the first User Defined Field (UDF1). Transfer of 56-octet cells must support the bandwidth requirements indicated in 2.5.

Table 2.1: 52 Octet Cell Format for 32-bit mode

Bit 31	Bit 23	Bit 15	Bit 0
Header 1	Header 2	Header 3	Header 4
Payload 1	Payload 2	Payload 3	Payload 4
:	:	:	:
:	:	:	:
Payload 45	Payload 46	Payload 47	Payload 48

Time

Table 2.2: 56 Octet Cell Format for 32-bit mode

Bit 31	Bit 23	Bit 15	Bit 0
Header 1	Header 2	Header 3	Header 4
UDF 1/HEC	UDF 2	UDF 3	UDF 4
Payload 1	Payload 2	Payload 3	Payload 4
:	:	:	:
:	:	:	:
Payload 45	Payload 46	Payload 47	Payload 48

Time

2.7.2 16-bit data path

When implementing the 16-bit interface the support for a 52-octet cell format as shown in Table 2.3 is required (**R**). The support for a 54-octet cell format as per Table 2.4 is optional (**O**). If transferring the HEC in the 54-octet cell format the HEC shall be transferred in the UDF1 field. Transfer of 54-octet cells must support the bandwidth requirements indicated in 2.5.

Table 2.3: 52 Octet Cell Format for 16-bit mode

Bit 15	Bit 0
Header 1	Header 2
Header 3	Header 4
Payload 1	Payload 2
:	:
Payload 47	Payload 48

Time

Table 2.4: 54 Octet Cell Format for 16-bit mode

Bit 15	Bit 0
Header 1	Header 2
Header 3	Header 4
UDF1/HEC	UDF2
Payload 1	Payload 2
:	:
Payload 47	Payload 48

Time

2.7.3 8-bit data path

When implementing the 8-bit interface the support for a 52-octet cell format as shown in Table 2.5 is required (**R**). The support for a 53-octet cell format as per Table 2.6 is optional (**O**). If transferring the HEC in the 53-octet cell format the HEC shall be transferred in the UDF1 field. Transfer of 53-octet cells must support the bandwidth requirements indicated in 2.5.

Table 2.5: 52 Octet Cell Format for 8-bit mode

Bit 7 Bit 0
Header 1
Header 2
Header 3
Header 4
Payload 1
:
:
Payload 48

Time

Table 2.6: 53 Octet Cell Format for 8-bit mode

Bit 7 Bit 0
Header 1
Header 2
Header 3
Header 4
UDF 1/HEC
Payload 1
:
:
Payload 48

Time

2.8 Decode-Response Timing

A device responds in two clock cycles after the initiating signal is sent across the interface. This deviates from Utopia Level 2 but relaxes timing constraints imposed on the responding device. The intent of this requirement is to have both input and output signals registered.

The exact timing for each of the operational modes will be described in the appropriate section.

3. Single PHY Interface

This section describes the operation of the Utopia Level 3 in Single PHY interface mode. In this configuration one ATM layer port and one PHY layer port will be connected.

3.1 Signals

Since this mode of operation only provides functionality to interface a single ATM port with a single PHY port the handshake requirements are minimal.

3.1.1 Transmit Interface

This section defines the signals required for the Transmit interface. These signals are the same signals as described in the Utopia Level 1 and 2 specifications, but are given for completeness.

The following signals are defined as required (**R**) for the Transmit interface:

TxClav[0]

> Cell Buffer Available. To indicate that space for at least one cell is available in the PHY transmit cell buffer.

TxEnb*

> Transmit Enable. The assertion of TxEnb* is coincident with the start of the cell transfer. TxEnb* is used for address selection in Multi-PHY mode during the last clock cycle before it is asserted.

TxSOC

> Transmit Start Of Cell. Active high signal asserted by the ATM layer to indicate the start of cell position. TxSOC is only asserted during the first clock cycle of the data transfer.

TxData[7:0]/TxData[15:0]/TxData[31:0]

> The data path for Transmit data, from ATM to PHY. In the 32-bit data path, TxData[31] is the MSB, TxData[0] is the LSB. In the 16-bit data path, TxData[15] is the MSB, TxData[0] is the LSB. Similarly, in the 8-bit data path, TxData[7] is the MSB and TxData[0] is the LSB.

TxClk

Transmit Clock, an input to both the ATM layer device and the PHY device. Used to clock the transmit control signals and data.

The following signal is defined as optional (**O**) for the Transmit interface:

TxPrty

Data path parity. The TxPrty parity bit serves as the odd parity bit over TxData[7:0]/TxData[15:0]/TxData[31:0].

3.1.2 Receive Interface

This section defines the signals required for the Receive interface. These signals are the same signals as described in the Utopia Level 1 and 2 specifications, but are given for completeness.

The following signals are defined as required (**R**) for the Receive interface:

RxClav[0]

Cell Available. To indicate that at least one cell is available in the PHY receive cell buffer.

RxEnb*

Receive Enable. Active low signal asserted by the ATM layer device to initiate a cell transfer. RxEnb* is used for address selection in Multi-PHY mode during the last clock cycle before it is asserted.

RxSOC

Receive Start Of Cell. Active high signal asserted by the PHY layer to indicate the start of cell position. RxSOC is only asserted during the first clock cycle of the data transfer.

RxData[7:0]/RxData[15:0]/RxData[31:0]

The data path for Receive data, from PHY to ATM. In the 32-bit data path, RxData[31] is the MSB, RxData[0] is the LSB. In the 16-bit data path, RxData[15] is the MSB, RxData[0] is the LSB. Similarly, in the 8-bit data path, RxData[7] is the MSB and RxData[0] is the LSB.

RxClk

Receive Clock, an input to both the ATM layer device and the PHY device. Used to clock the receive control signals and data.

The following signal is defined as optional (**O**) for the Receive interface:

RxPrty

Data path parity. The RxPrty parity bit serves as the odd parity bit over RxData[7:0]/RxData[15:0]/RxData[31:0].

3.2 Direct Status Indication

The Single PHY mode of operation only uses a single TxClav and RxClav signal and no address information, since there is only 1 port to receive cell data from or send cell data to. The transfer of a cell, once started, cannot be stalled or interrupted. RxEnb* and TxEnb* must be held low until required to pause the transfer of the next cell.

3.2.1 Transmit Operation

The ATM layer device can send a cell to a PHY port only when the PHY port has indicated to the ATM layer device that it is ready to receive at least one cell. The PHY device will indicate this by asserting the Transmit Cell Buffer Available (TxClav). The TxClav signal is not applicable on the first cycle after Start of Cell because of the 2 clock cycle decode-response timing. Thereafter the PHY device will deassert TxClav unless it can accept at least 1 cell (after the currently transferred cell) from the ATM layer device. Once the TxClav has been asserted, it will have to stay asserted until the clock edge after assertion of the next Start of Cell (SOC).

Figure 3.1 shows the case in which cells are transferred back-to-back, utilizing the full bandwidth of the bus.

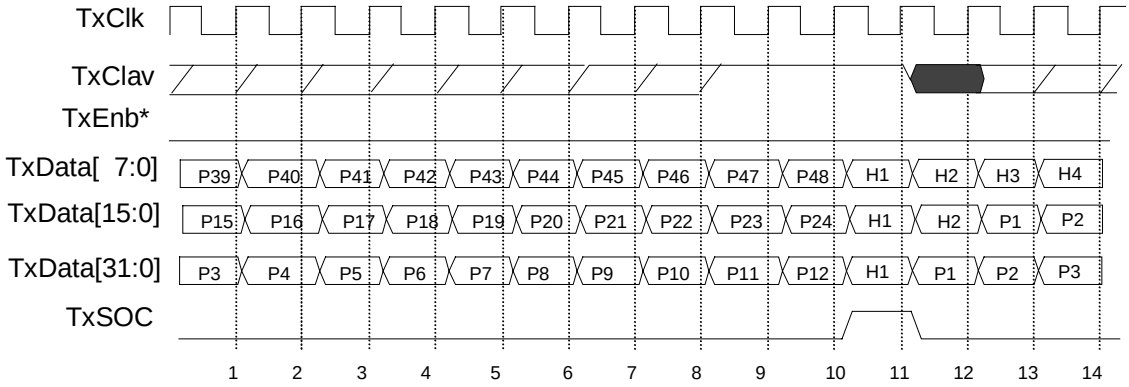


Figure 3.1: Transmission of two cells back-to-back

Figure 3.2 shows an example where the PHY indicates on clock edge 4 that it can accept another cell but the ATM layer device does not have a cell ready for transfer. When ready, the ATM layer will assert the TxSOC and start transmission of the cell simultaneously (clock cycle n).

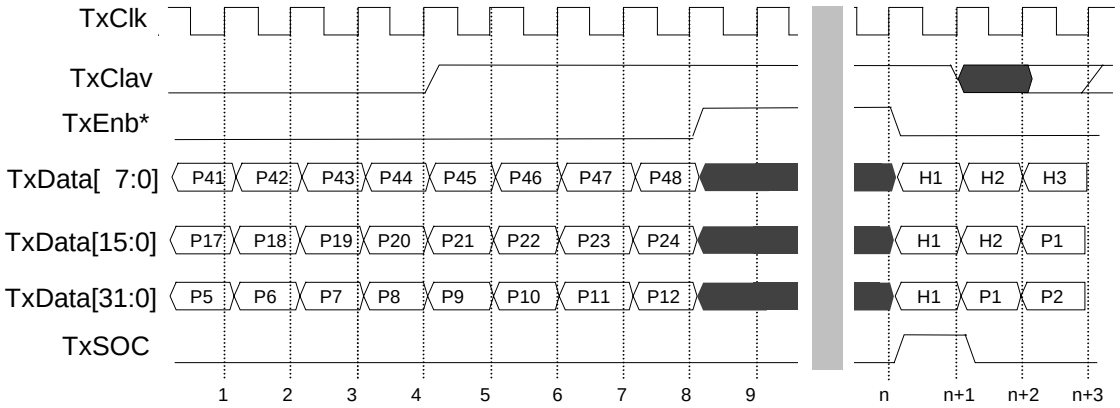


Figure 3.2: Transmission stalled by the ATM layer device

In Figure 3.3 the PHY indicates that it has no space available for a complete cell by deasserting the TxClav. In response to this, the ATM layer will hold off the transmission of the next cell (even if it has a cell available for transmission). Once TxClav is asserted by the PHY and the ATM device has a cell available for transfer, TxSOC will be asserted and transfer takes place.

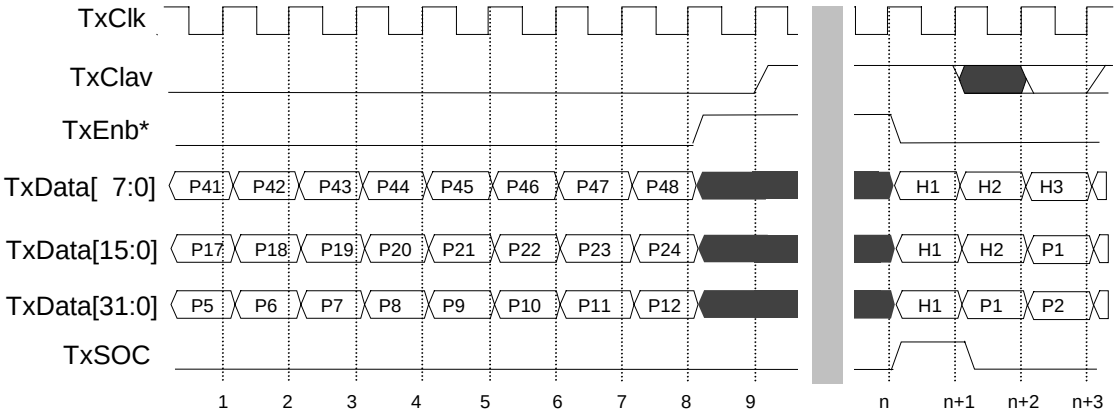


Figure 3.3: PHY layer device not ready to receive cell

3.2.2 Receive Operation

The PHY layer device can send a cell to a ATM port only when PHY port has indicated that it has at least one complete ATM cell available and when the ATM port has indicated to the PHY layer device that it is ready to receive a cell. The ATM device will indicate this by asserting the RxEnb* in response to a Receive Cell Available (RxClav) signal from the PHY device. During the transfer of a cell the status of the RxClav signal indicates the availability of a subsequent cell. The ATM device must deassert RxEnb* two cycles before the end of the cell transfer, unless a back-to-back transfer is intended. The RxClav must be deasserted coincident with RxSOC if the PHY has no subsequent cell available. Once the RxClav has been asserted, it will have to stay asserted until the next Start of Cell (SOC) is asserted.

Figure 3.4 shows the case in which cells are transferred back-to-back by keeping RxEnb* asserted at the next to the last cycle of the transfer, utilizing the full bandwidth of the bus.

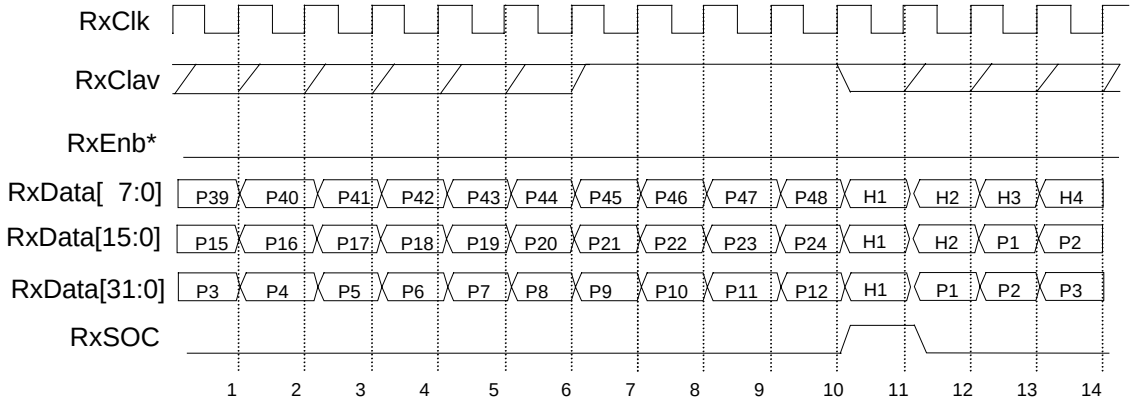


Figure 3.4: Reception of two cells back-to-back

Figure 3.5 shows an example where the PHY layer device indicates on clock edge 4 or before that it has another complete cell available but the ATM layer device does not have space available to receive this cell. To indicate this, the ATM layer deasserts RxEnb* until it has space available for a complete cell. The timing of the RxEnb* signal is pipelined, which means that the response of the PHY port is two clock cycles after the RxEnb* is asserted or deasserted.

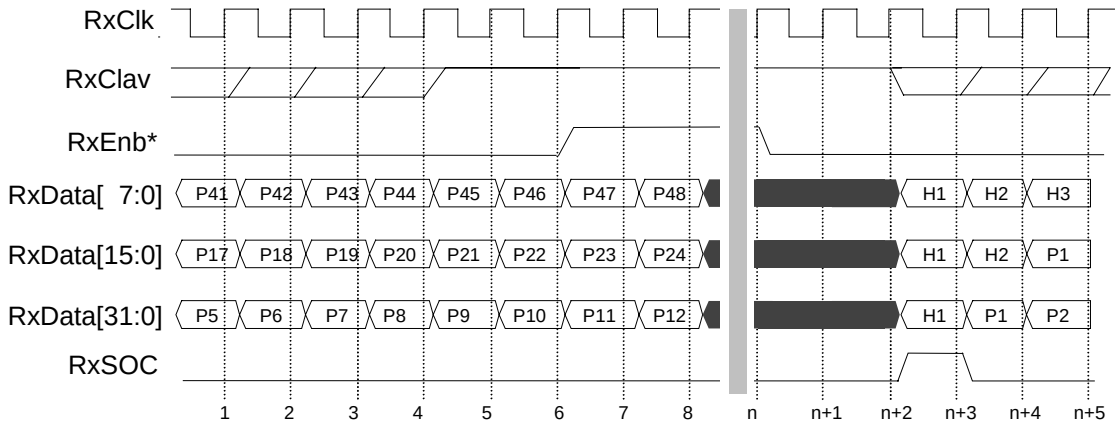


Figure 3.5: Reception stalled by the ATM layer device

In Figure 3.6 the PHY indicates that it does not have a complete cell available for transfer across the Utopia Level 3 interface by deasserting the RxClav. In response to this, the ATM layer device will deassert the RxEnb*. Once RxClav is asserted by the PHY and the ATM device has space available for a complete cell, the PHY will be selected by the ATM layer device (RxEnb* asserted) and transfer takes place. The PHY layer device will place the cell data on the RxData bus two clock cycles after the assertion of the RxEnb*.

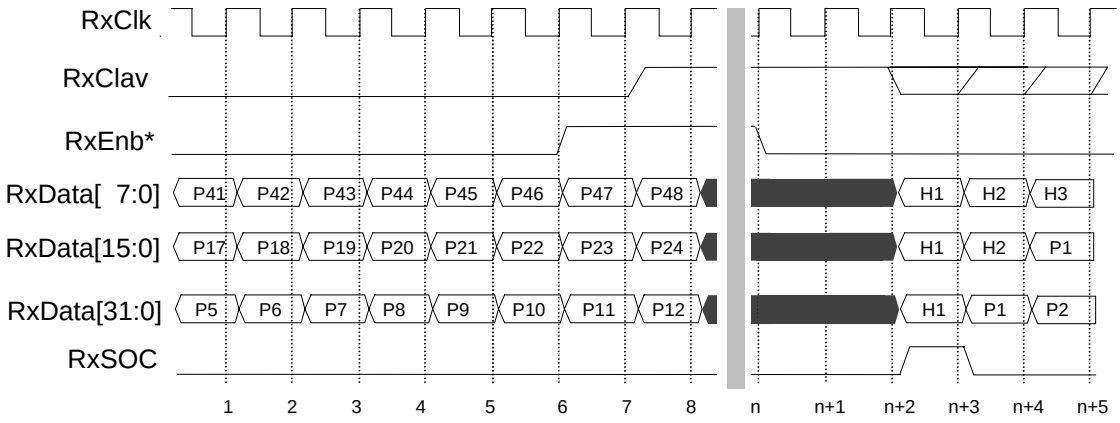


Figure 3.6: PHY layer device not ready to transmit cell

4. Data Path Operation – MPHY mode

This section describes the operation of the Utopia Level 3 in MPHY interface mode. In this configuration one ATM layer port and multiple PHY layer ports will be connected.

4.1 Signals

The data path in MPHY mode consists of the same signals as described in the previous section, with the MPHY specific additional signals described below.

4.1.1 Transmit Interface

This section defines the additional signals required for the Transmit interface to operate in MPHY mode.

The following signals are defined as required (**R**) for the Transmit interface operating in MPHY mode:

TxAddr[n:0]

> Transmit Address. To select the PHY port for which the transmit data is to be destined. The address is used in both Direct Status indication mode and the Single Clav (polling) mode. The value of n is application specific. All 2^{n+1} addresses are available for use in the application as no NULL address is supported.

The following signals are defined as optional (**O**) for the Transmit interface operating in MPHY mode:

TxClav[3:1]

> Cell Buffer Available. To indicate that space for at least one cell is available in the PHY transmit cell buffer. These signals are only required in Direct Status Indication operation.

4.1.2 Receive Interface

This section defines the additional signals required for the Receive interface to operate in MPHY mode.

The following signals are defined as required (**R**) for the Receive interface operating in MPHY mode:

RxAddr[n:0]

Receive Address. To select the PHY port from which receive data is to be read. The address is used in both Direct Status indication mode and the Single Clav (polling) mode. The value of n is application specific. All 2^{n+1} addresses are available for use in the application as no NULL address is supported.

The following signals are defined as optional (**O**) for the Receive interface operating in MPHY mode:

RxClav[3:1]

Cell Available. To indicate that at least one cell is available in the PHY receive cell buffer. These signals are only required in Direct Status Indication operation.

4.2 Direct Status Indication

When interfacing up to 4 PHY ports to a single ATM layer device, it is possible to implement a dedicated RxClav and TxClav signal for each of the PHY ports. The mode of operation in this scenario is called “Direct Status Indication”. The meaning and timing of the individual TxClav and RxClav signals is as described in section 3.2, Direct Status Indication for the Single PHY Interface.

Timing diagrams are shown in Figure 4.1 to 4.6 to illustrate the transmit and receive timing of the signals involved in MPHY Direct Status Indication.

4.2.1 Transmit Operation

The ATM layer device can send a cell to a PHY port only when the PHY port has indicated to the ATM layer device that it is ready to receive at least one complete cell. The PHY device must indicate transmit cell buffer available information to the ATM layer device. The TxClav[3:0] is not applicable on the first cycle after Start of Cell because of the 2 clock cycle decode-response timing. Thereafter the PHY device will deassert TxClav unless it can accept at least 1 cell (after the currently transferred cell) from the ATM layer device. This is illustrated in Figure 4.1 by the TxClav[3:0] indicating the status of each of the PHY transmit ports. Once the TxClav[3:0] has been asserted, it will have to stay asserted until the clock edge after assertion of the next Start of Cell (SOC) on that particular port.

The PHY port to which the next cell will be sent will be selected by TxAddr[n:0] during the clock cycle before TxEnb* is asserted. This signal will be decoded by the PHY device and the specified port will be ready to receive cell data from the ATM side as soon as the TxEnb* is asserted.

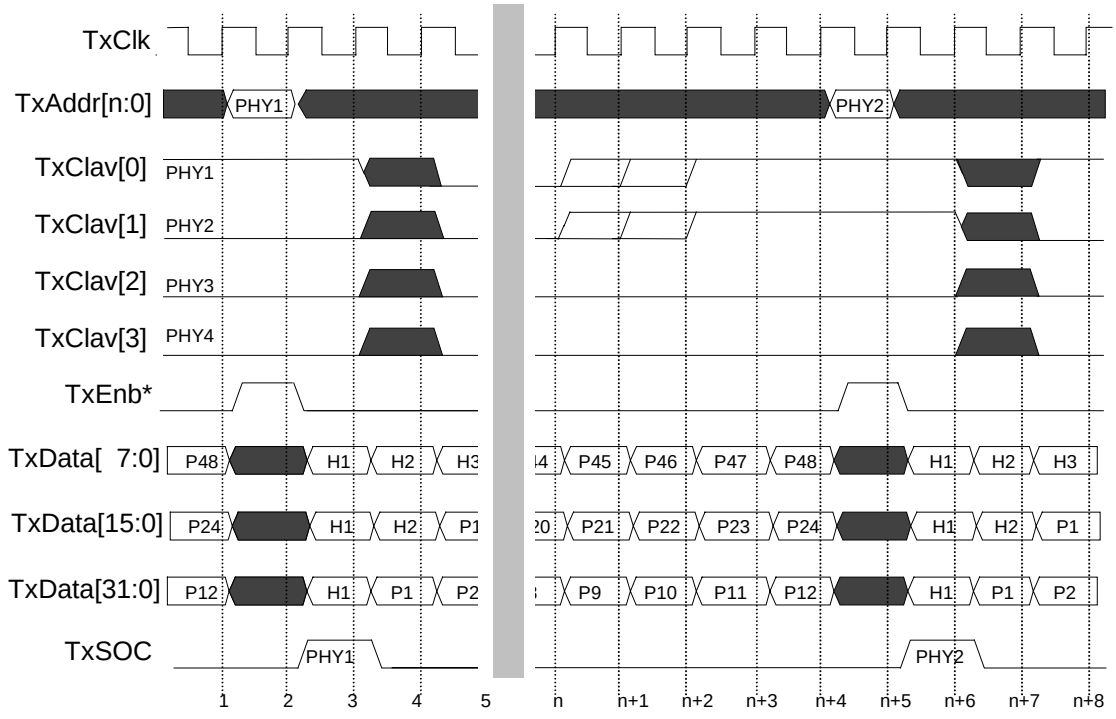
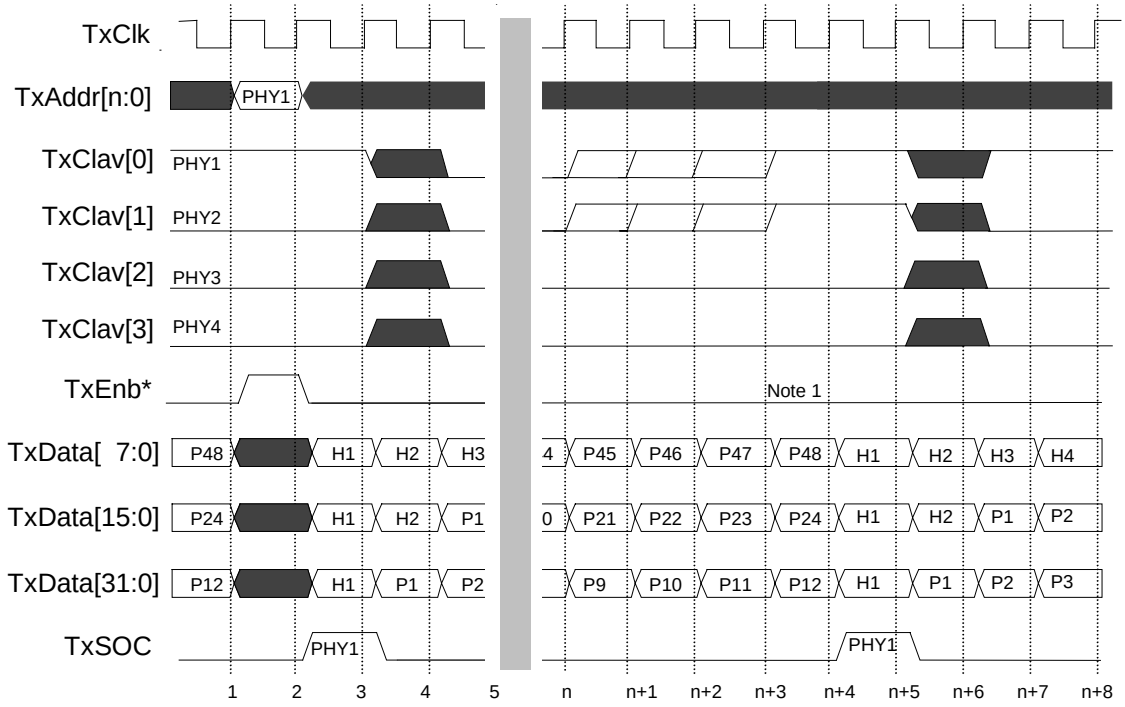


Figure 4.1: Transmit Decode and Selection

Back-to-back transfer of cells is possible when two cells have to be sent to the same port and this port indicates that it can receive the second cell. In the case of back-to-back transfer the ATM layer device does not explicitly select the PHY port and TxEnb* will not be deasserted. The second (or subsequent) cell is transferred immediately after the previous one and the TxSOC is asserted to indicate the start of cell. This is illustrated in Figure 4.2.



Note 1: Implicit re-selection of PHY1 occurs on clock edge n+4 since TxEnb* remains asserted.

Figure 4.2: Back-to-back cell transmission

In Figure 4.3 the PHY indicates that none of its ports has space available for a complete cell by deasserting the TxClav[3:0]. This causes the ATM layer to deassert the TxEnb* as soon as the current transfer has finished (clock cycle 8). Once a TxClav is asserted by the PHY and the ATM device has a cell available for transfer to this port, the PHY port will be selected by the ATM layer (TxAddr[n:0] during the clock cycle before asserting TxEnb*) and transfer is started as soon as TxEnb* is asserted (clock cycle n+1).

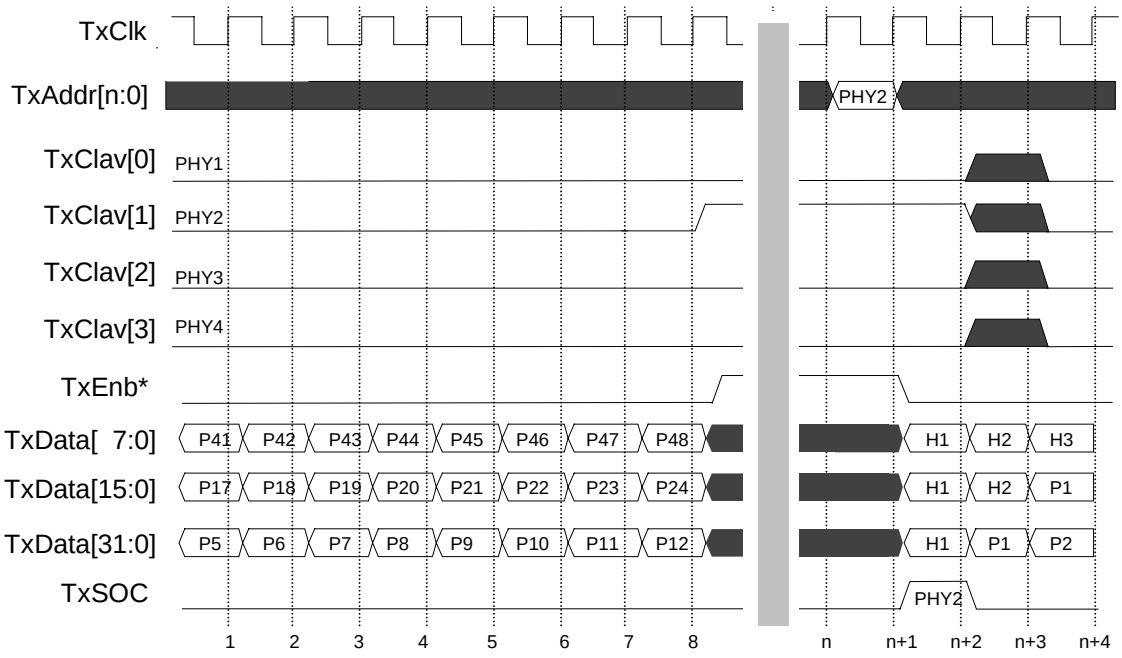


Figure 4.3: PHY layer device not ready to receive cell

4.2.2 Receive Operation

In the receive direction, the ATM layer device controls the flow of data from the PHY device on a per cell basis. The PHY device must indicate receive cell available information to the ATM layer device. The ATM layer device can only explicitly select (or implicitly reselect) a PHY port for transfer of a cell when the PHY port has indicated to the ATM layer device that it has at least one cell available. This is illustrated in Figure 4.4 by the RxClav[3:0] indicating the status of each of the PHY receive ports. The RxClav[3:0] must be deasserted coincident with RxSOC to indicate that the corresponding port of the PHY has no subsequent cell available. Once the RxClav[3:0] has been asserted, it will have to stay asserted until the Start of Cell (SOC) is asserted (clock edge 4 in Figure 4.4) on that particular port.

A valid RxAddr[n:0] during the clock cycle before asserting the RxEnb* signal will select the PHY port which will transfer the next cell across the Utopia interface. This signal will be decoded by the PHY device and the specified port will be ready to transfer cell data two clock cycles after RxEnb* goes low. The ATM device must deassert RxEnb* two cycles before the end of the cell transfer, unless a back-to-back transfer is intended. The decode-response timing between the RxEnb* and the RxData is therefore two clock cycles.

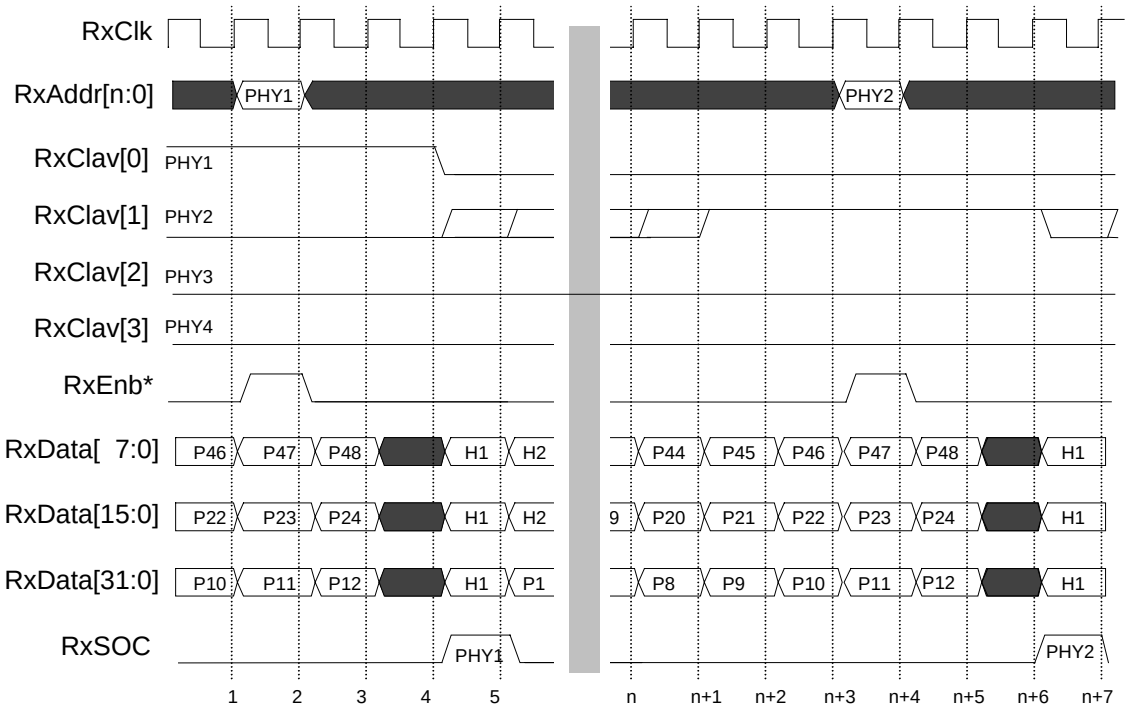
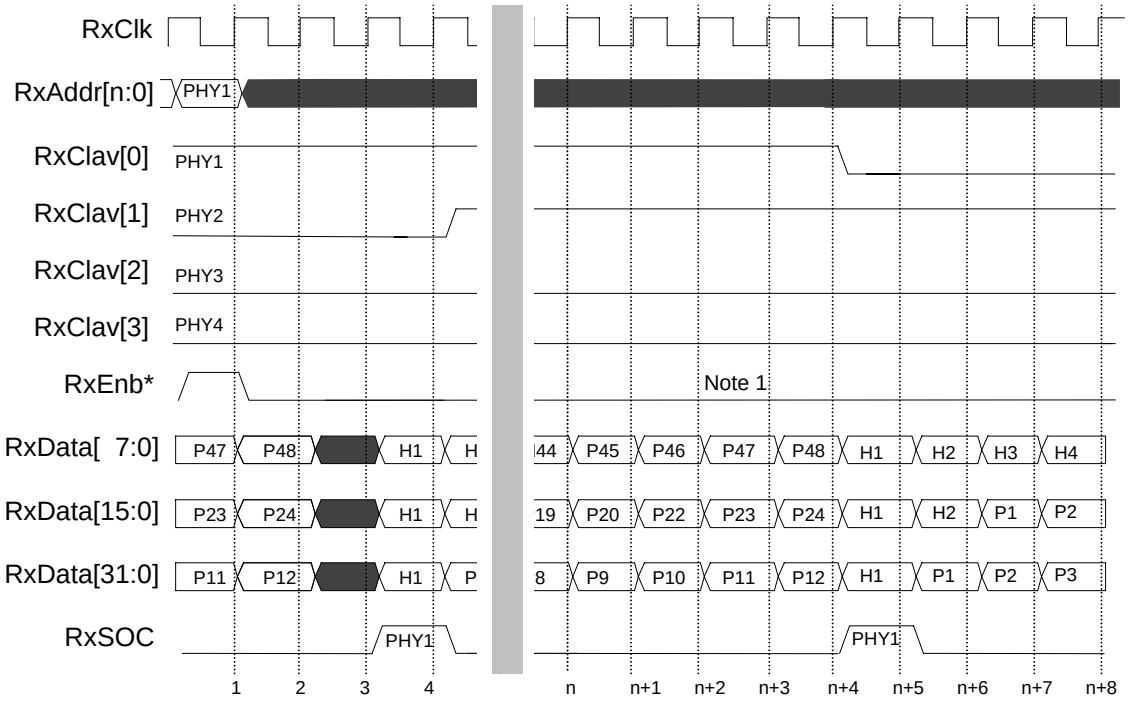


Figure 4.4: Receive Decode and Selection

Back-to-back transfer of cells is possible when the PHY layer device indicates in time that it has another cell to be transferred from the same port and the ATM layer device can receive this cell. In the case of back-to-back transfer the ATM layer device implicitly reselects the PHY port by leaving the RxEnb* asserted during the next to the last cycle of the cell transfer. The second (or subsequent) cell is transferred immediately after the previous one and the RxSOC is asserted to indicate the start of cell. This is illustrated in Figure 4.5.



Note 1: Implicit re-selection of PHY1 occurs on clock edge n+3 since RxEnb* remains asserted.

Figure 4.5: Back-to-back cell transfer

In Figure 4.6 the PHY indicates that none of its ports has a complete cell available for transfer by deasserting all RxClav signals. As a response to this, the ATM layer will deassert the RxEnb* to indicate that no cell transfer will take place after the current transfer is completed. Once a RxClav is asserted by the PHY and the ATM device has space available to receive a cell, the PHY port will be selected by a valid RxAddr[n:0] during the clock cycle before asserting the RxEnb* and transfer takes place two clock cycles after the RxEnb* has been asserted.

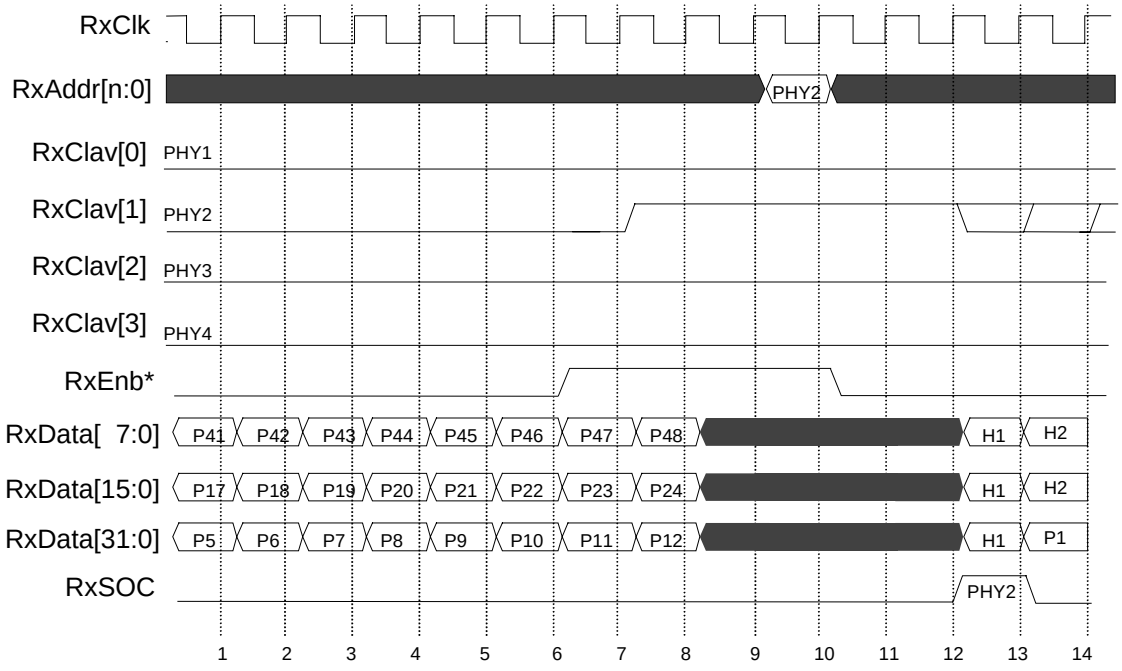


Figure 4.6: PHY layer device not ready to send cell

4.3 Multi-PHY Operation with 1 TxClav & 1 RxClav Signal

4.3.1 General operation

The ATM layer device receives PHY port FIFO status information through the following polling mechanism:

In the transmit direction, the ATM layer device polls by presenting the PHY's port address on TxAddr[n:0]. The polled PHY responds two cycles later by driving TxClav high if the port can accept one or more complete ATM cells; TxClav is driven low otherwise.

In the receive direction, the ATM layer device polls by presenting the PHY's port address on RxAddr[n:0]. The polled PHY responds two cycles later by driving RxClav high if the port is ready to send one or more complete ATM cells to the ATM layer device; RxClav is driven low otherwise.

4.3.2 Back-to-back polling

The single Clav mode described in this section is very similar to the mechanism described in the Utopia Level 2 specification. However, due to the elimination of the tri-state requirement in Utopia Level 3, it is possible to poll the PHY ports back-to-back. This means that in both transmit and receive directions, the ATM layer device may successively poll PHY ports on contiguous cycles.

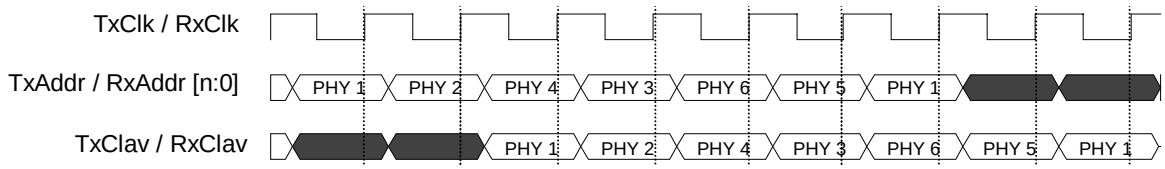


Figure 4.7: Back-to-back Polling.

4.3.3 Transmit Operation

The ATM layer device can send a cell to a PHY port only when the PHY port has indicated to the ATM layer device that it is ready to receive at least one cell. The PHY device must send transmit cell buffer available information for that port to the ATM layer device when that port is polled, using the TxClav. Once the TxClav response for a particular port indicates buffer availability, responses to subsequent polls of that port must continue to indicate buffer availability until after the second cycle of the transfer of a cell to that port.

This is illustrated in Figure 4.8 by the TxClav indicating the status of the PHY transmit port two clock cycles after the port's address has been selected by the ATM device. The decode-response timing between the TxAddr and the TxClav is therefore two clock cycles. The TxClav is not applicable on the first cycle after Start of Cell because of the 2 clock cycle decode-response timing.

TxAddr[n:0] during the clock cycle before asserting the TxEnb* signal will select the PHY port which will receive the next cell. The PHY device will decode this signal and the specified port will be ready to receive cell data from the ATM side at the next clock cycle.

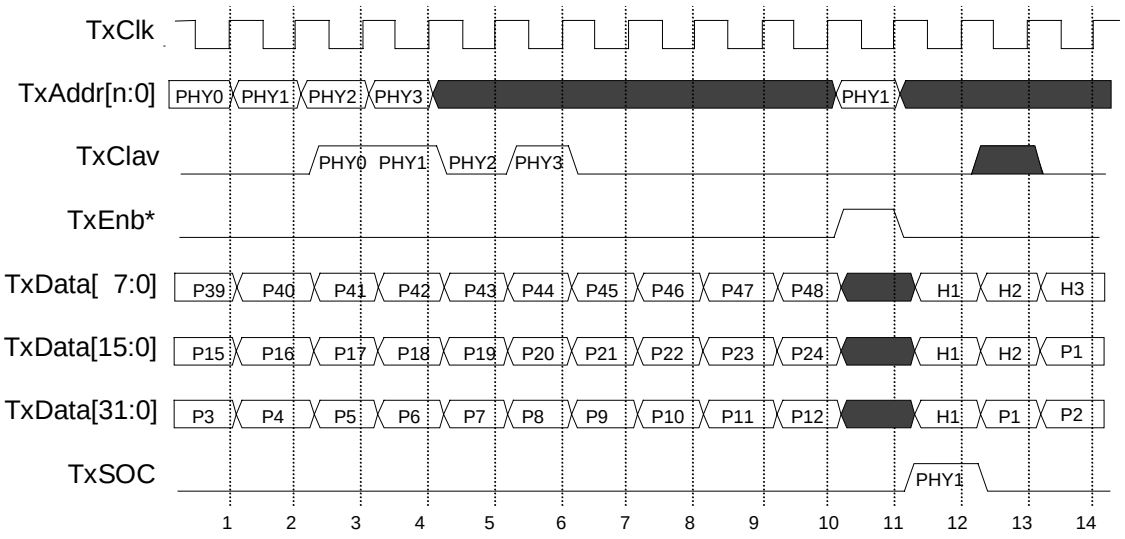
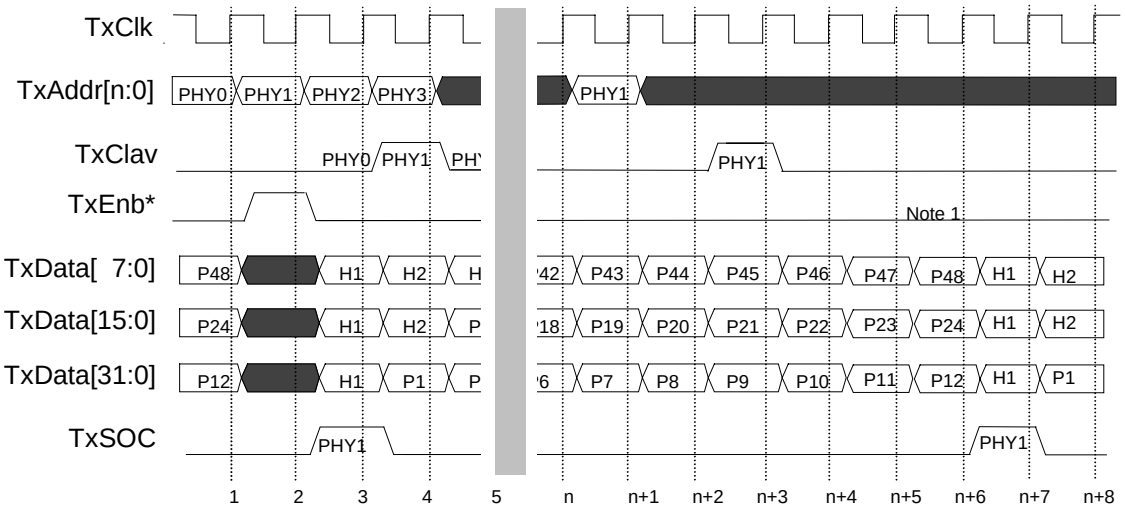


Figure 4.8: Transmit Decode and Selection

Back-to-back transfer of cells is possible when two cells have to be sent to the same Multi-PHY device port and this port indicates that it can receive the second cell. In the case of back-to-back transfer the ATM layer device implicitly reselects the PHY port by leaving the TxEnb* asserted during the next to the last cycle of the cell transfer. The second (or subsequent) cell is transferred immediately after the previous one and the TxSOC is asserted to indicate the start of cell. This is illustrated in Figure 4.9.



Note 1: Implicit re-selection of PHY1 occurs on clock edge n+6 since TxEnb* remains asserted.

Figure 4.9: Back-to-back transmission of cells

4.3.4 Receive Operation

In the receive direction, the ATM layer device controls the flow of data from the PHY device on a per cell basis. The ATM layer device can explicitly select (or implicitly reselect) a PHY port for transfer of a cell only when the PHY port has indicated to the ATM layer device that it has at least one cell available, using the RxClav.

The explicit case is illustrated in Figure 4.10 by the RxClav indicating the status of the PHY receive port two clock cycles after the port's address has been selected by the ATM device. The decode-response timing between the RxAddr and the RxClav is therefore two clock cycles. Once the RxClav response for a particular port indicates cell availability, responses to subsequent polls of that port must continue to indicate cell availability until the Start Of Cell (SOC) is asserted for that port.

RxAddr[n:0] during the clock cycle before asserting the RxEnb* signal will select the PHY port which will transfer the next cell across the Utopia interface. The PHY device will decode this signal and the specified port will be ready to transfer cell data two clock cycles after RxEnb has gone low. The ATM device must deassert RxEnb* two cycles before the end of the cell transfer, unless a back-to-back transfer is intended. The decode-response timing between the RxEnb and the RxData is therefore two clock cycles.

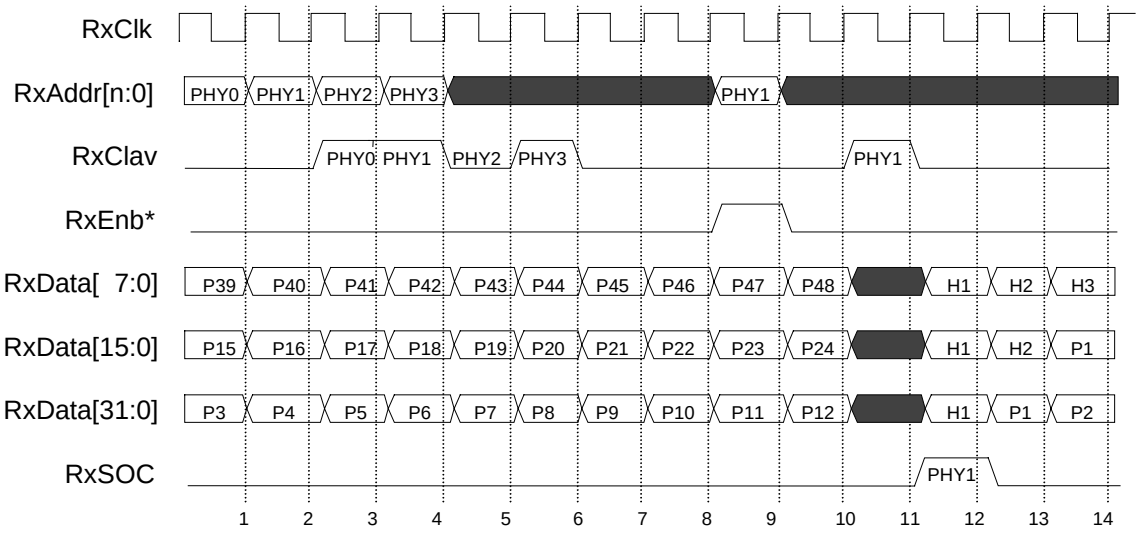
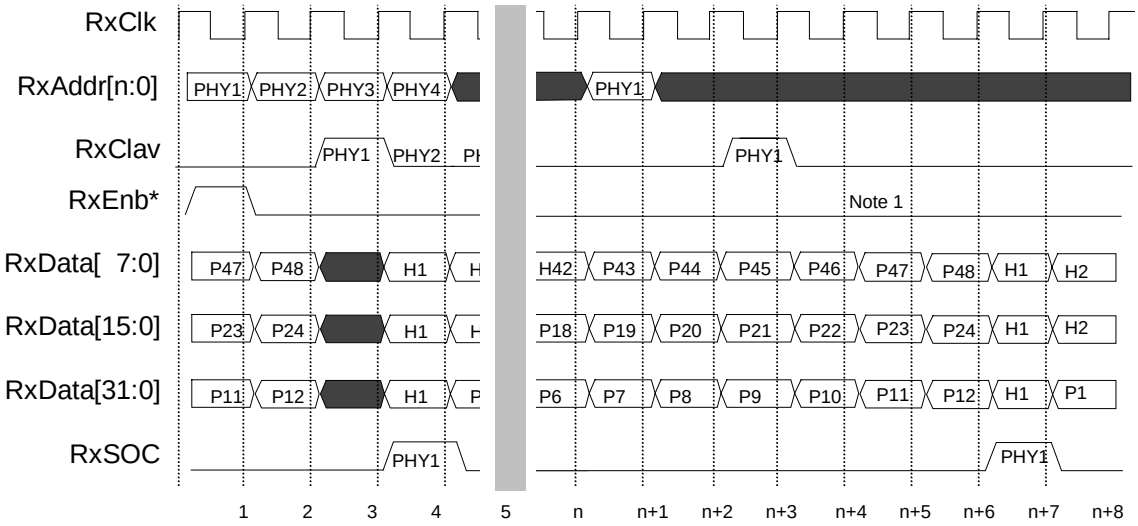


Figure 4.10: Receive Decode and Selection

Back-to-back reception of cells is possible when two or more cells have to be received from the same port and the ATM layer device can receive the second cell. In this case of back-to-back transfer the ATM layer device does not explicitly select the PHY port as transfer to the same port is assumed. The second (or subsequent) cell is transferred immediately after the previous one and the RxSOC is asserted to indicate the start of cell. This is illustrated in Figure 4.11.



Note 1: Implicit re-selection of PHY1 occurs on clock edge n+5 since RxEnb* remains asserted.

Figure 4.11: Back-to-back transfer of cells from PHY to ATM

5. Timing Details

5.1 A.C characteristics

The A.C. characteristics are based on the timing specification for the receiver side of a signal. The setup and hold times are defined with regard to a positive clock edge, see Figure 5.1.

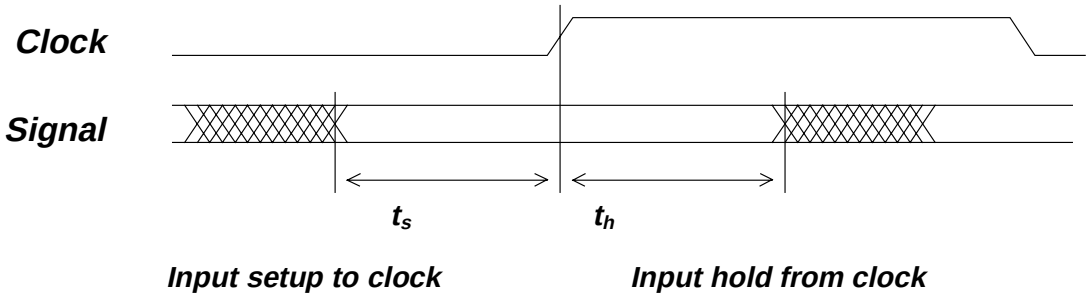


Figure 5.1: Setup and Hold time definition

Table 5.1 lists the AC characteristics for the Utopia Level 3 interface. The Test Conditions are the standard resistor and capacitor terminations used in standard logic devices. Utopia Level 3 is specified such that all inputs and outputs are registered. Thus, the inputs have setup and hold times specified and the outputs have clock-to-output times specified.

Table 5.1: AC Characteristics

AC Specifications with Supply Voltage, V_{dd} = 3.0 V to 3.6 V

Sym	Parameter	Test Condition	Min	Typ	Max	Unit
f_{clk}	Clock Frequency				104	MHz
t_{PHL} t_{PLH}	Clock to Output	25 pf, 500 Ω, All Outputs			6.0	ns
t_s	Input Setup Time	All Inputs	2.0			ns
t_h	Input Hold Time	All Inputs	0.5			ns
t_{pw}	Clock Pulse Width	High or Low	4.0			ns

Pulse Generator for all test pulses: Rate = 2.0MHz; t_r = 1.5 ns; t_f = 1.5 ns.

5.2 D.C. characteristics

The following Tables 5.2A and 5.2B list the DC characteristics for the Utopia Level 3 interface. The parameters are for point-to-point connection of devices that are within reasonable distances of each other, minimizing transmission line effects. The two tables both show the DC characteristics, with Table 5.2A giving the values as a percentage of the power supply voltage, while Table 5.2B gives the absolute values. Meeting the conditions set out in either table ensures compliance with the Utopia Level 3 specification DC characteristics. However, the method given in table 5.2A is the preferred method.

Table 5.2A: DC Characteristics specification, relative values

DC Specifications with Supply Voltage, V_{dd} = 3.0 V to 3.6 V

Sym	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	High-level Output Voltage	I_{OH} = -8 mA	0.8 V_{dd}			V
V_{IH}	High-level Input Voltage		0.65 V_{dd}			V
	Nominal Switching Point			$V_{dd}/2$		V
V_{IL}	Low-level Input Voltage				0.35 V_{dd}	V
V_{OL}	Low-level Output Voltage	I_{OL} = 8 mA			0.2 V_{dd}	V
I_{IN}	Input Current - Inputs Only	V_{IN} = 0 or V_{IN} = V_{dd}			+/-5	µA
	Input Current - I/O Terminals				+/-15	

Old fixed DC CMOS TTL Specification method for 3.3 volt logic.

Table 5.2B: DC Characteristics, absolute values

DC Specifications with Supply Voltage, V_{dd} = 3.0 V to 3.6 V

Sym	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	High-level Output Voltage	I_{OH} = -8 mA	2.4			V
V_{IH}	High-level Input Voltage		2.0			V
	Nominal Switching Point					V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OL}	Low-level Output Voltage	I_{OL} = 8 mA			0.4	V
I_{IN}	Input Current - Inputs Only	V_{IN} = 0 or V_{IN} = V_{dd}			+/-5	µA
	Input Current - I/O Terminals				+/-15	

CMOS devices specified with fixed DC voltages will inter-operate with CMOS devices specified with percent-of-Vdd voltages (% Vdd). The design of these IC's is usually identical and only the specification method is different (Old JEDEC form versus new JEDEC form). If in doubt about specific products, contact the manufacturer.

5.3 Absolute Maximum Ratings

The following table lists the Absolute Maximum Ratings for the Utopia Level 3 devices.

Table 5.3: Absolute Maximum Ratings

Sym	Rating	Max Range	Unit
V_{TERM}	Input and Vcc terminals with respect to GND	-0.5 to +4.6	V
V_{TERM}	Output and I/O terminals with respect to GND	-0.5 to +4.6	V
T_A	Operating Temperature	-40 to +85	°C
T_{BIAS}	Bias Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C

6. Data Path Signal Summary

This is a complete signal list for both transmit and receive data paths.

6.1 Transmit Interface Signals

Table 6.1: Transmit Interface Signals

Signal	Direction	Req./Opt	Description
TxAddr[n:0]	ATM to PHY	R for MPHY	Address of MPHY device being selected
TxData[7:0] TxData[15:0] TxData[31:0]	ATM to PHY	R	Data bus in 8-bit mode Data bus in 16-bit mode Data bus in 32-bit mode
TxPrty	ATM to PHY	O	Data bus odd parity
TxSOC	ATM to PHY	R	Start Of Cell
TxEnb*	ATM to PHY	R	Enables port selection in MPHY mode
TxClav[0]	PHY to ATM	R	Cell Buffer Available
TxClav[3..1]	PHY to ATM	O	Cell Buffer Available (for MPHY Direct Status Indication)
TxClk	Input	R	Transfer/interface clock

6.2 Receive Interface Signals

Table 6.2: Receive Interface Signals

Signal	Direction	Req./Opt	Description
RxAddr[n:0]	ATM to PHY	R for MPHY	Address of MPHY device being selected
RxData[7:0] RxData[15:0] RxData[31:0]	PHY to ATM	R	Data bus in 8-bit mode Data bus in 16-bit mode Data bus in 32-bit mode
RxPrty	PHY to ATM	O	Data bus odd parity
RxSOC	PHY to ATM	R	Start Of Cell
RxEnb*	ATM to PHY	R	Enable data transfers; enables port selection in MPHY mode
RxClav[0]	PHY to ATM	R	Cell Available
RxClav[3..1]	PHY to ATM	O	Cell Available (for MPHY Direct Status Indication)
RxClk	Input	R	Transfer/interface clock

Appendix 1. References

[1] ATM Forum Technical Committee, AF-PHY-0017.000, “Utopia, An ATM-PHY Interface Specification, Level 1, Version 2.01”, March 21, 1994

[2] ATM Forum Technical Committee, AF-PHY-0039.000, “Utopia Level 2, Version 1.0”, June 1995