CS4232

Games Compatible Plug-and-Play Audio System

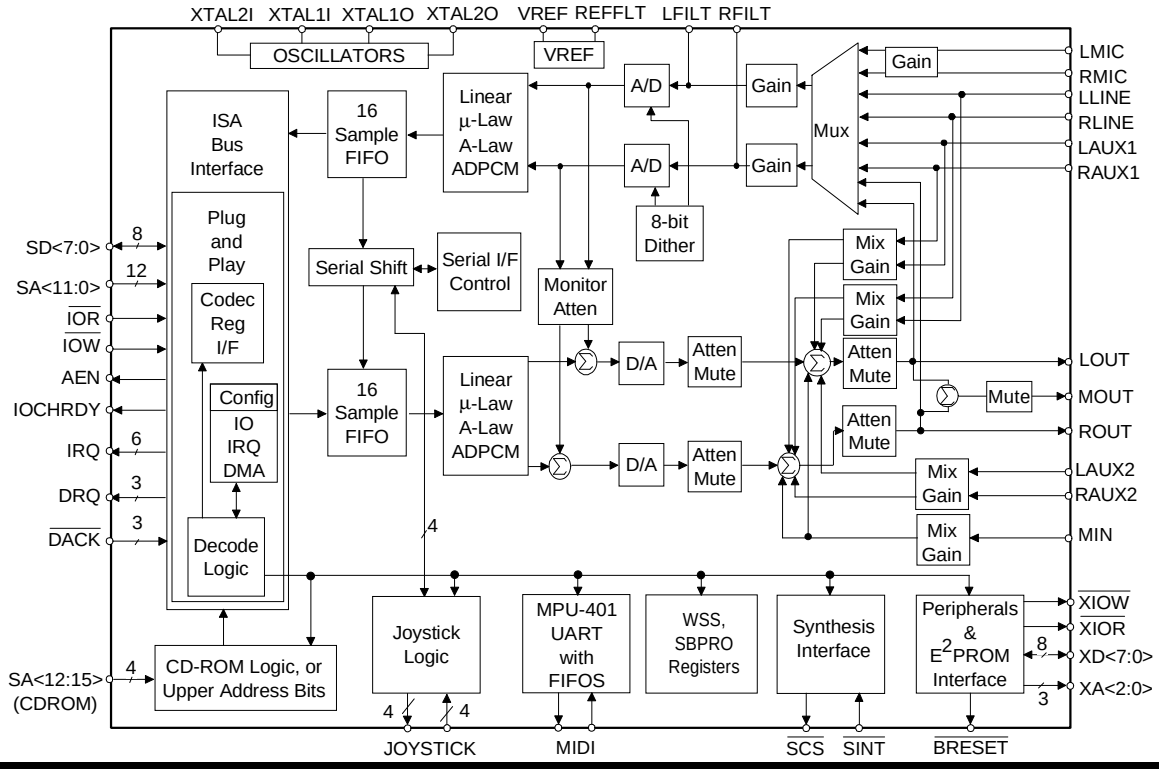
- Compatible with Sound Blaster™, Sound Blaster Pro™, and Windows Sound System™
- Fully Plug and Play Compatible
- Industry Leading Delta-Sigma Data Converters
- ADPCM, μ-Law & A-Law Compression/Decompression
- Dual DMA Support w/FIFOs, Full Duplex Operation
- MPC Level-2 Compatible Mixer
- Joystick Port and MPU-401 Compatible MIDI Interface
- Optional CD-ROM Interface
- External FM and Wave Table Synthesizer Support
- Serial Audio Data Port
- 24 mA TTL Bus Drive Capability
- Software Programmable Power Management
- 16-Bit Address Decode Support
- CS4231/CS4248 Register Compatible

General Description

The CS4232 is a single chip multimedia audio system controller and codec that provides compatibility with ISA Plug and Play, the Microsoft Windows Sound System, and will run software written to the Sound Blaster and Sound Blaster Pro interfaces. The CS4232 integrates an industry-standard Delta-Sigma codec with extended signal processing in a high-performance mixed-signal design. The CS4232 also contains expansive mixing capabilities, an MPU-401 UART, joystick logic, and interfaces for a music synthesizer and a CD-ROM.

ORDERING INFORMATION:

CS4232-KQ	100 pin TQFP, 14x14x1.4mm
CS4232-KM	100 pin PQFP, 14x20x2.3mm



Advanced Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25 °C; VA, VD1-VD2, VDF1-VDF3 = +5V;
Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD2; 1 kHz Input Sine wave; Sample Frequency, Fs = 48 kHz;
Measurement Bandwidth is 10 Hz to 20 kHz, 16-bit linear coding.)

Parameter*		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum Gain Setting (0dB); unless otherwise specified.						
ADC Resolution	(Note 1)		16			Bits
ADC Differential Nonlinearity	(Note 1)				±0.5	LSB
Instantaneous Dynamic Range	Line Inputs (Note 2) Mic Inputs	IDR	80 72	83 79		dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD		0.006 0.01	0.02 0.025	% %
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs Line-to-AUX1 Line-to-AUX2			80 80 90 90		dB dB dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs				±0.5 ±0.5	dB dB
Programmable Input Gain Span	Line Inputs		21.5	22.5		dB
Gain Step Size			1.3	1.5	1.7	dB
ADC Offset Error	0 dB gain			±10	±100	LSB
Full Scale Input Voltage:	(MGE=1) MIC Inputs (MGE=0) MIC Inputs LINE, AUX1, AUX2, MIN Inputs		0.26 2.6 2.6	0.28 2.8 2.8		V_{pp} V_{pp} V_{pp}
Gain Drift				±100		ppm/°C
Input Resistance	(Note 1)		20			kΩ
Input Capacitance	(Note 1)				15	pF

Notes: 1. This specification is guaranteed by characterization, no production testing.
2. MGE = 1 (see WSS Indirect Reg I0, I1) and a 10 µF capacitor on the VREF pin.

*Parameter definitions are given at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*			Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation (0dB); unless otherwise specified.							
DAC Resolution		(Note 1)		16			Bits
DAC Differential Nonlinearity		(Note 1)				±0.5	LSB
Dynamic Range	-Total -Instantaneous	All Outputs	TDR IDR	 80	95 85		dB dB
Total Harmonic Distortion		(Note 3)	THD		0.01	0.02	%
Interchannel Isolation	Line Out	(Note 3)			95		dB
Interchannel Gain Mismatch		Line Out			±0.1	±0.5	dB
Voltage Reference Output - VREF				2.0	2.2	2.3	V
Voltage Reference Output Current - VREF		(Notes 1,4)			100	400	µA
DAC Programmable Attenuation Span				93	94.5		dB
DAC Attenuation Step Size		0 dB to -81 dB -82.5 dB to -94.5 dB		1.3 1.0	1.5 1.5	1.7 2	dB dB
DAC Offset Voltage					±1	±10	mV
Full Scale Output Voltage:	OUT, MOUT	(Note 3)		2.6	2.9	3.2	V_{pp}
Gain Drift					100		ppm/°C
Deviation from Linear Phase		(Note 1)				1	Degree
External Load Impedance				10			kΩ
Mute Attenuation (0 dB)				80			dB
Total Out-of-Band Energy	0.6xFs to 100 kHz	(Note 1)				-45	dB
Audible Out-of-Band Energy	0.6xFs to 22 kHz	(Fs=8kHz) (Note 1)				-70	dB
Power Supply							
Power Supply Current		Digital, Operating Analog, Operating Total Digital, Power Down Analog, Power Down			61 41 102 50 50	110 60 170 200 200	mA mA mA µA µA
Power Supply Rejection	1 kHz	(Note 1)		40			dB

Notes: 3. 10 kΩ, 100 pF load.

4. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.

MIXERS (T_A = 25 °C; VA, VD1-VD2, VDF1-VDF3 = +5V; Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD2; 1 kHz Input Sine wave)

Parameter		Symbol	Min	Typ	Max	Units
Mixer Gain Range Span	LINE, AUX1, AUX2 MIN Master		45 42 26	46.5 45 30		dB dB dB
Step Size	LINE, AUX1, AUX2 MIN Master		1.3 2.3 1.6	1.5 3.0 2.0	1.7 3.4 2.4	dB dB dB

ABSOLUTE MAXIMUM RATINGS (AGND, DGND, SGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital Analog	VD1-VD2 VDF1-VDF3 VA1,VA2	-0.3 -0.3 -0.3	6.0 6.0 6.0	V V V
Total Power Dissipation	(Supplies, Inputs, Outputs)			1	W
Input Current per Pin	(Except Supply Pins)		-10.0	+10.0	mA
Output Current per Pin	(Except Supply Pins)		-50	+50	mA
Analog Input Voltage			-0.3	VA+0.3	V
Digital Input voltage			-0.3	VD+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND, SGND = 0V, all voltages with repect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital Digital Filtered Analog	VD1-VD2 VDF1-VDF3 VA	4.75 4.75 4.75	5.0 5.0 5.0	5.25 5.25 5.25	V V V
Operating Ambient Temperature		T_A	0	25	70	°C

DIGITAL FILTER CHARACTERISTICS (Note 1)

Parameter	Symbol	Min	Typ	Max	Units
Passband		0		0.40xFs	Hz
Frequency Response		-1.0		+0.5	dB
Passband Ripple (0-0.40xFs)				±0.1	dB
Transition Band		0.40xFs		0.60xFs	Hz
Stop Band		0.60xFs			Hz
Stop Band Rejection		74			dB
Group Delay 8- and 16-bit formats Stereo ADPCM format Mono ADPCM format				10/Fs 14/Fs 18/Fs	s s s
Group Delay Variation vs. Frequency ADCs DACs				0.0 0.1/Fs	µs µs

DIGITAL CHARACTERISTICS (T_A = 25°C; VA, VD1-VD2, VDF1-VDF3 = 5V; AGND, DGND1-DGND2, SGND1-SGND3 = 0V.)

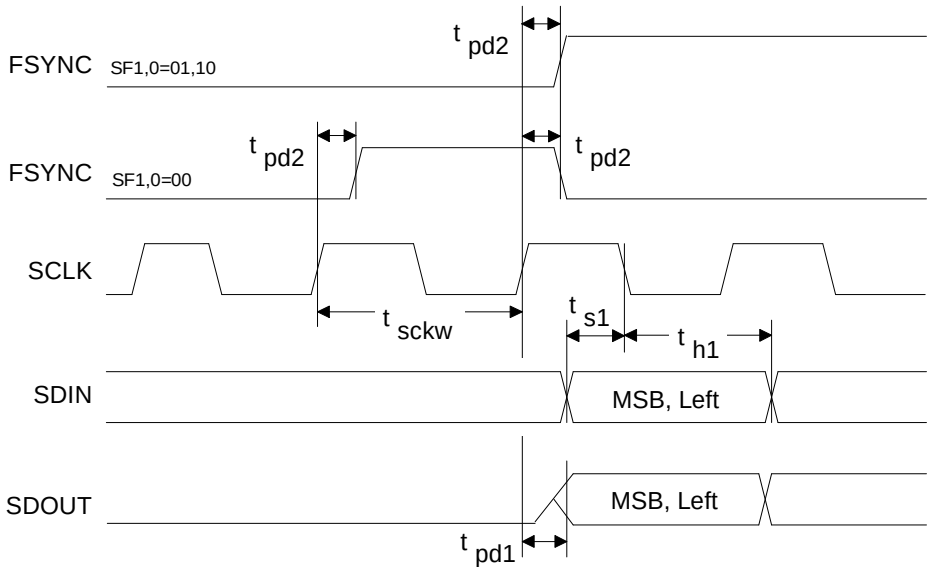
Parameter		Symbol	Min	Max	Units
High-level Input Voltage	Digital Inputs XTAL1I/XTAL2I	V_{IH}	2.0 VD-1.0	VD+0.3 VD+0.3	V V
Low-level Input Voltage		V_{IL}	-0.3	0.8	V
High-level Output Voltage:	ISA Bus Pins I_0 = -24.0 mA IOCHRDY, SDA/XD0 (Note 7) All Others I_0 = -1.0 mA	V_{OH}	2.4 2.4	VD VD	V V
Low-level Output Voltage:	ISA Bus Pins I_0 = 24.0 mA IOCHRDY I_0 = 8.0 mA All Others I_0 = 4.0 mA	V_{OL}		0.4 0.4 0.4	V V V
Input Leakage Current	(Digital Inputs)		-10	10	µA
Output Leakage Current	(High-Z Digital Outputs)		-10	10	µA

Note 7. Open Collector pins. High level output voltage dependent on external pull up (required) used and number of peripherals (gates) attached.

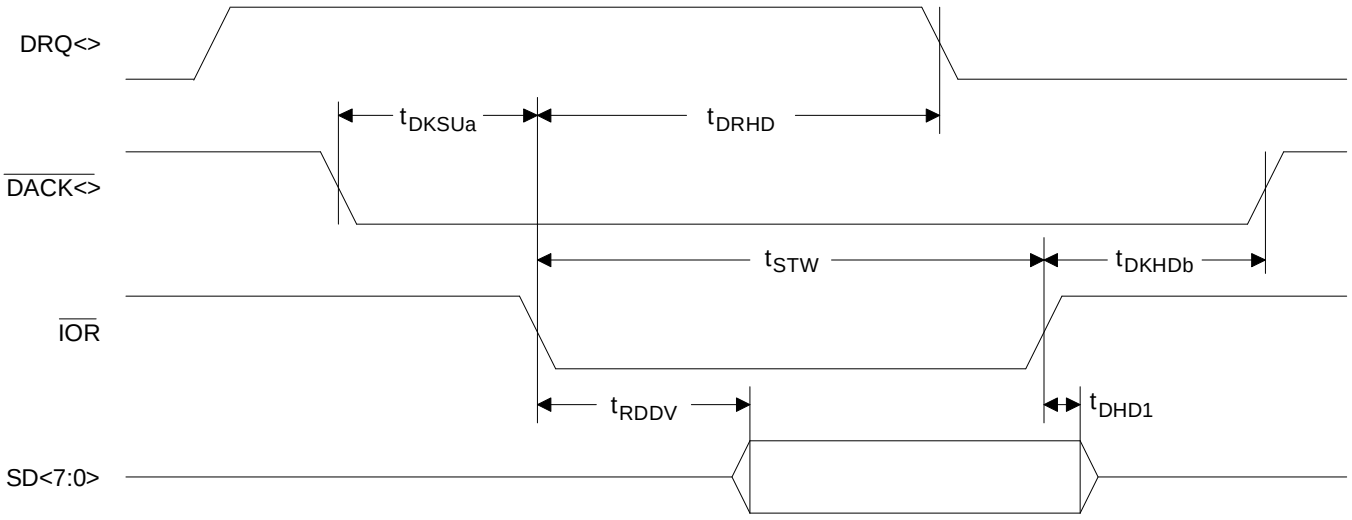
TIMING PARAMETERS (T_A = 25 °C; VA, VD1-VD2, VDF1-VDF3 = +5V; outputs loaded with 30pF Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD2)

Parameter	Symbol	Min	Max	Units
$\overline{IOW}$ or $\overline{IOR}$ strobe width	t_{STW}	90		ns
Data valid to $\overline{IOW}$ rising edge (write cycle)	t_{WDSU}	22		ns
$\overline{IOR}$ falling edge to data valid (read cycle)	t_{RDDV}		60	ns
SA <> and AEN setup to $\overline{IOR}$ or $\overline{IOW}$ falling edge	t_{ADSU}	22		ns
SA <> and AEN hold from $\overline{IOW}$ or $\overline{IOR}$ rising edge	t_{ADHD}	10		ns
$\overline{DACK}$<> inactive to $\overline{IOW}$ or $\overline{IOR}$ falling edge (DMA cycle immediately followed by a non-DMA cycle) (Note 11)	t_{SUDK1}	60		ns
$\overline{DACK}$<> active from $\overline{IOW}$ or $\overline{IOR}$ rising edge (non-DMA cycle completion followed by DMA cycle) (Note 11)	t_{SUDK2}	0		ns
$\overline{DACK}$<> setup to $\overline{IOR}$ falling edge (DMA cycles) $\overline{DACK}$<> setup to $\overline{IOW}$ falling edge (Note 11)	t_{DKSUa} t_{DKSUb}	25 25		ns ns
Data hold from $\overline{IOW}$ rising edge	t_{DHD2}	15		ns
$\overline{DRQ}$<> hold from $\overline{IOW}$ or $\overline{IOR}$ falling edge DTM(I10) = 0 (assumes no more DMA cycles needed) DTM(I10) = 1	t_{DRHD}	 -25	45	ns
Time between rising edge of $\overline{IOW}$ or $\overline{IOR}$ to next falling edge of $\overline{IOW}$ or $\overline{IOR}$	t_{BWDN}	80		ns
Data hold from $\overline{IOR}$ rising edge	t_{DHD1}	0	25	ns
$\overline{DACK}$<> hold from $\overline{IOW}$ rising edge $\overline{DACK}$<> hold from $\overline{IOR}$ rising edge	t_{DKHDa} t_{DKHDb}	25 25		ns ns
RESDRV pulse width high	t_{RESDRV}	40		ms
XTAL1I, XTAL2I frequency (Notes 1,8,9)			25.6	MHz
XTAL1I, XTAL2I high time (Notes 1,9)		18		ns
XTAL1I, XTAL2I low time (Notes 1,9)		18		ns
Sample Frequency (Note 1)	Fs	3.918	50	kHz
Serial Port Timing				
SCLK frequency (Note 10)	t_{SCLKW}		Fsx64	Hz
SCLK rising to SDOUT valid	t_{PD1}		30	ns
SCLK rising to FSYNC transition	t_{PD2}	-20	20	ns
SDIN valid to SCLK falling	t_{S1}	30		ns
SDIN hold after SCLK falling	t_{H1}	30		ns

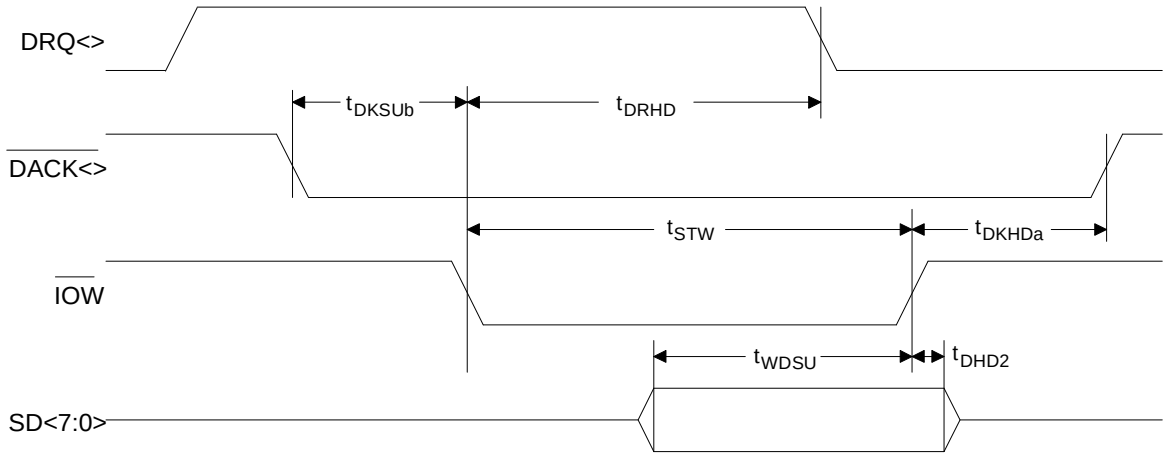
Notes: 8. The higher frequency crystal should be placed on XTAL1 which is designed for higher loop gains.
9. The Sample frequency specification must not be exceeded.
10. When SF1,0 = 10, 32-bit mode, SCLK is active for the first 32 bit periods of the frame, and remains low during the last 32 bit periods of the frame.
11. AEN must be high during DMA cycles.



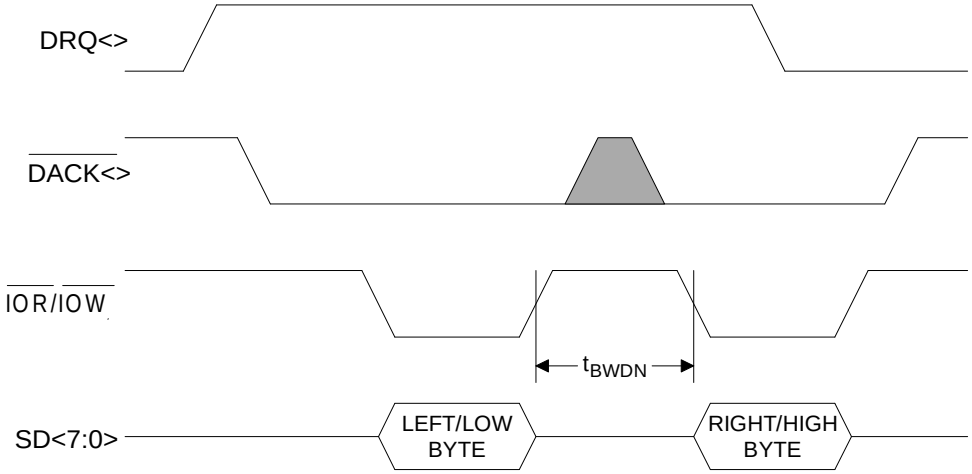
Serial Port Timing



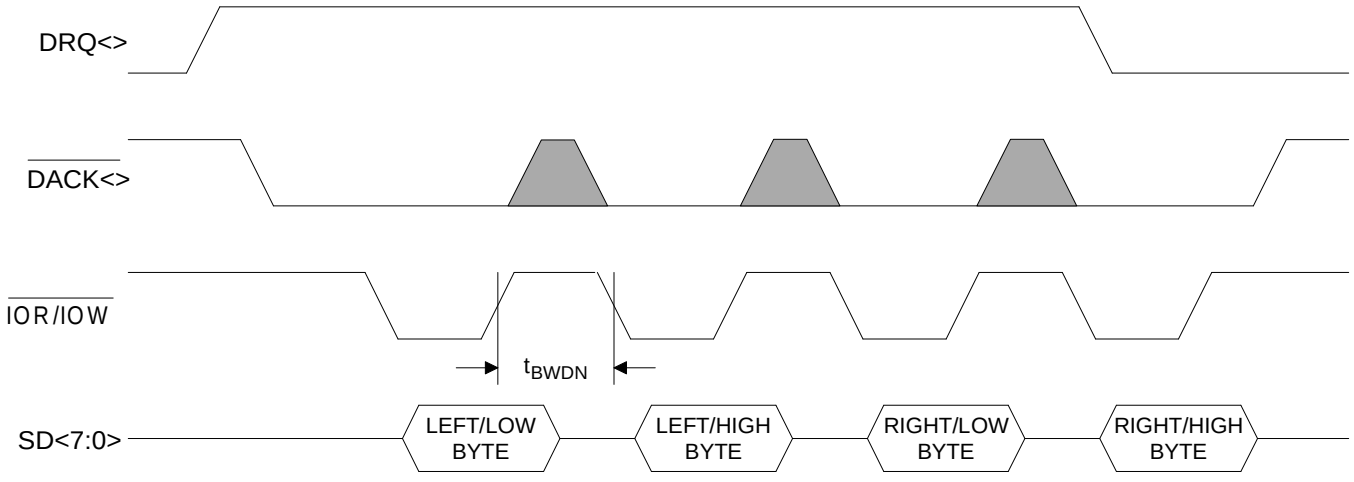
8-Bit Mono DMA Read/Capture Cycle



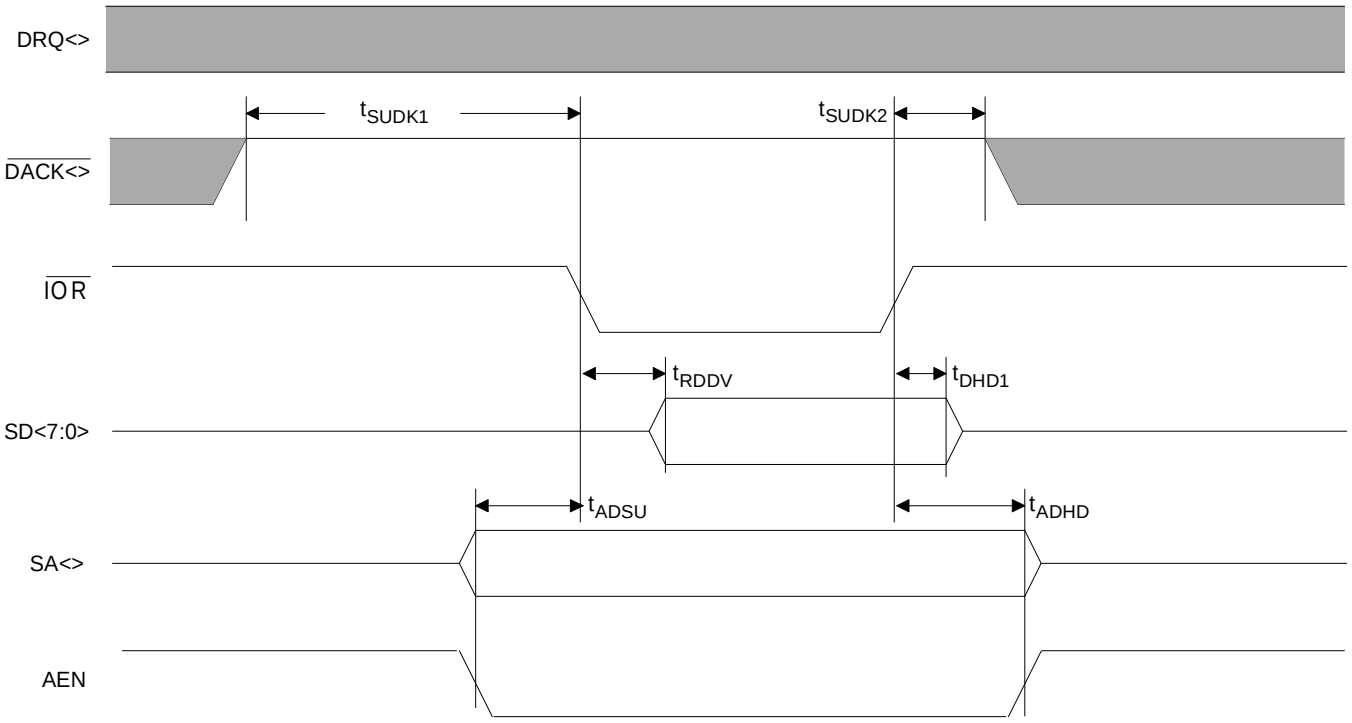
8-Bit Mono DMA Write/Playback Cycle



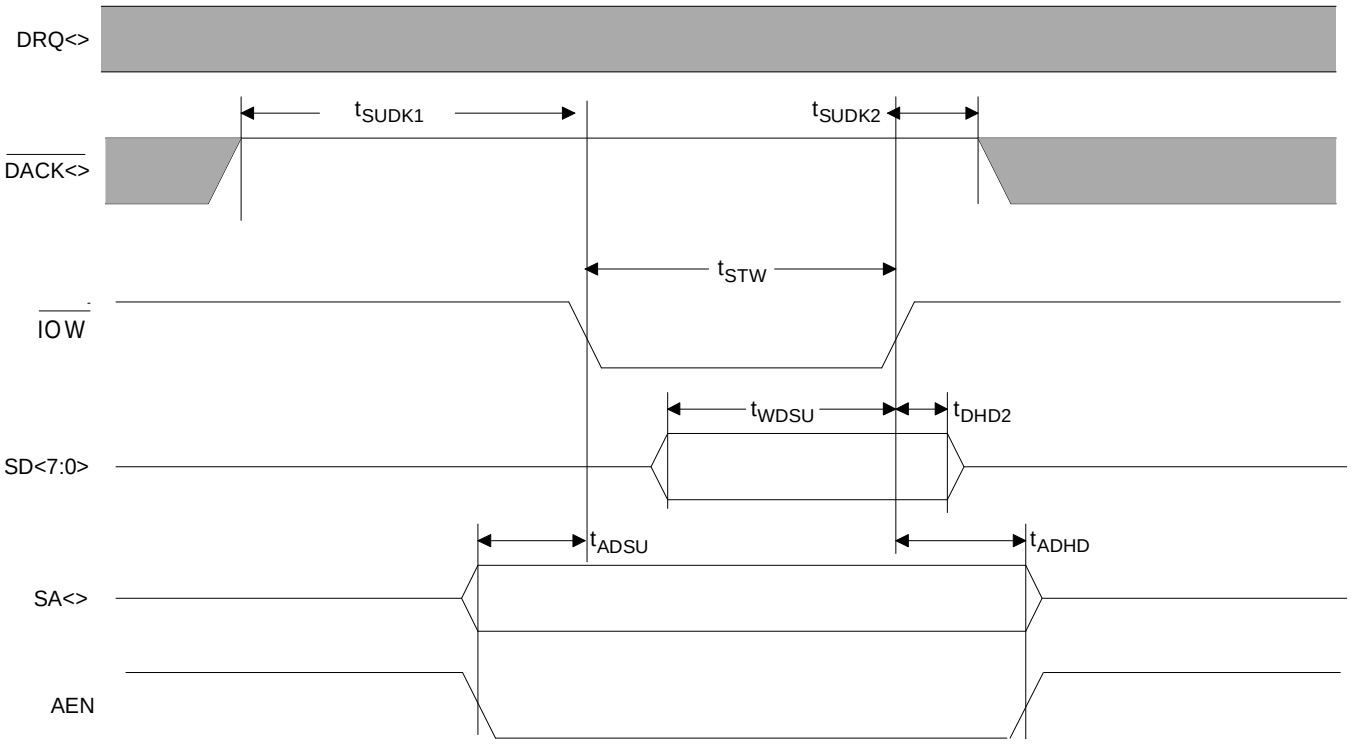
8-Bit Stereo or 16-Bit Mono DMA Cycle



16-Bit Stereo or ADPCM DMA Cycle



I/O Read Cycle



I/O Write Cycle

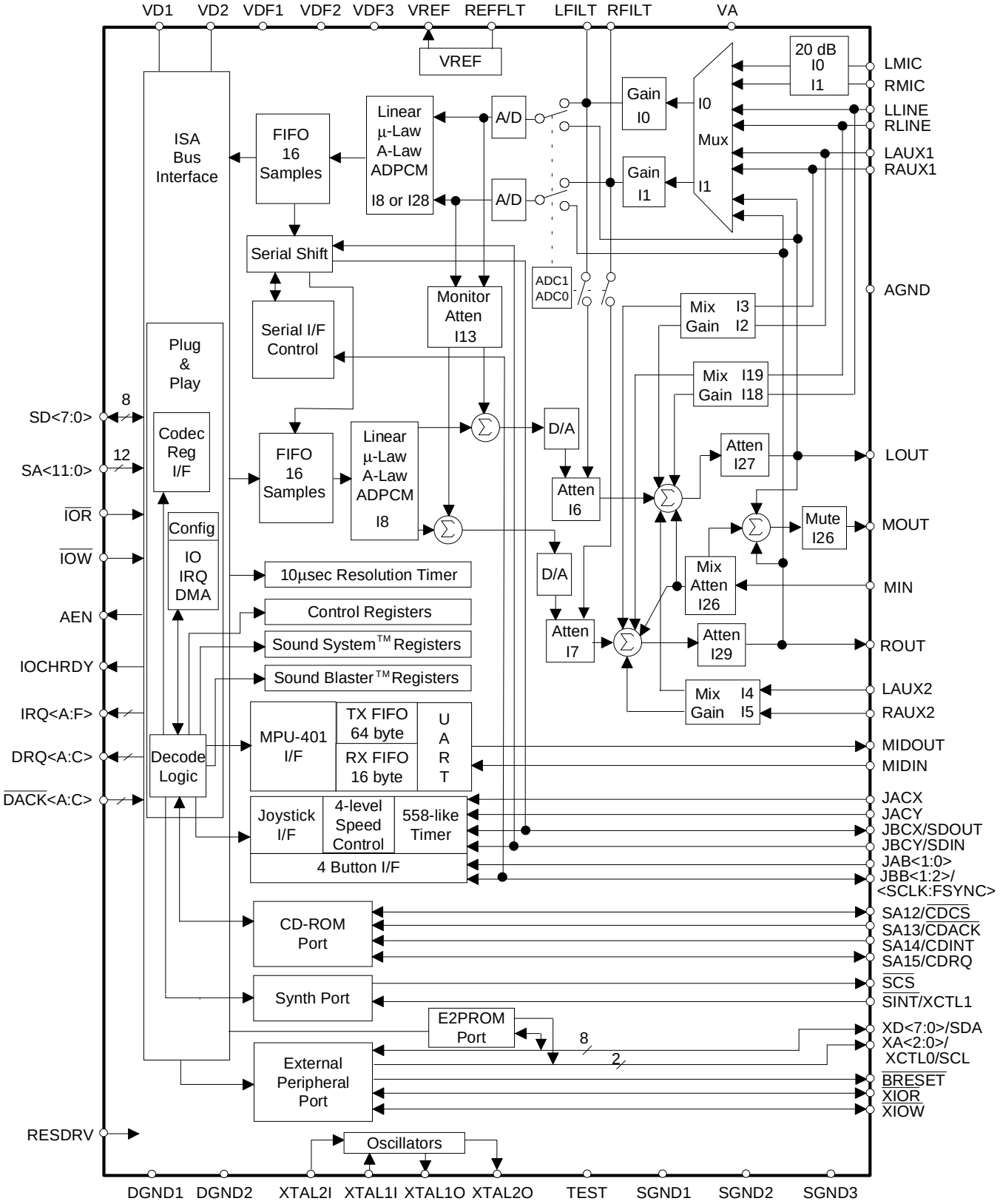


Figure 1. CS4232 Block Diagram

GENERAL DESCRIPTION

The CS4232 is comprised of five physical devices along with Plug-and-Play support for two additional external devices. The internal devices are:

Windows Sound System Codec
Sound Blaster Pro Compatible Interface
Game Port (Joystick)
Control
MPU-401

The two external devices are:

Synthesizer
CDROM

In addition, the CS4232 includes a full ISA interface with Plug and Play compatibility and an External Peripheral Port for interfacing to external devices (i.e. Synthesizer and CDROM). Since the Synthesizer and CDROM analog inputs are external, mapping as shown in Figure 3, on page 44, must be used to maintain Sound Blaster compatibility, i.e. FM analog must be connected to the LINE analog inputs of the codec. A Karaoke mode has also been added to the CS4232 where the Mic input can be mixed into the output mixer. The bits to control this mode are found in the Control logical device interface on page 47.

When initially powered up, the CS4232 IC is isolated from the bus, and each device supported by the CS4232 must be activated via software. Once activated, each device responds to the resources given (Address, IRQ, and DMA channels). The seven devices listed above are grouped into 5 logical devices, as shown in Figure 2. Bracketed features are supported, but typically not used. The five logical devices are:

LOGICAL DEVICE 0:
Windows Sound System Codec (WSS Codec)
Synthesizer
Sound Blaster Pro Compatible Interface

LOGICAL DEVICE 1: Game Port

LOGICAL DEVICE 2: Control

LOGICAL DEVICE 3: MPU401

LOGICAL DEVICE 4: CDROM

Logical Device 0 consists of three physical devices. The WSS Codec and the Synthesizer are grouped together since the original Windows Sound System board expected an FM synthesizer if the codec was present. The Sound Blaster Pro Compatible interface, SBPro, is also grouped to allow the WSS Codec and the SBPro to share Interrupts and DMA channels. The Synthesizer device is externally located on the Peripheral Port and could be an FM synthesizer such as the OPL3, or a wave table synthesizer such as the CS9233. The WSS Codec and the SBPro compatible devices are internal to the CS4232 IC.

Logical Device 1 is the Game Port that supports up to two joystick devices.

Logical Device 2 is the Control device that supports global features of the CS4232 IC. This device uses I/O locations to control power management, joystick rate, and PnP resource data loading.

Logical Device 3 is the MPU401 interface. The MPU401 MIDI interface includes a 64-byte FIFO for data transmitted out the MIDOUT pin and a 16-byte FIFO for data received from the MIDIN pin.

Logical Device 4 supports a CDROM connected to the peripheral port. This interface, on the external peripheral port, can support CDROMs with up to 8 I/O locations, an interrupt, and a DMA channel. Although this logical device is listed as a CDROM, any external device that fits within the resources listed above may be substituted. If the CDROM port is used for another device, the PnP resource data must be updated to reflect the new device.

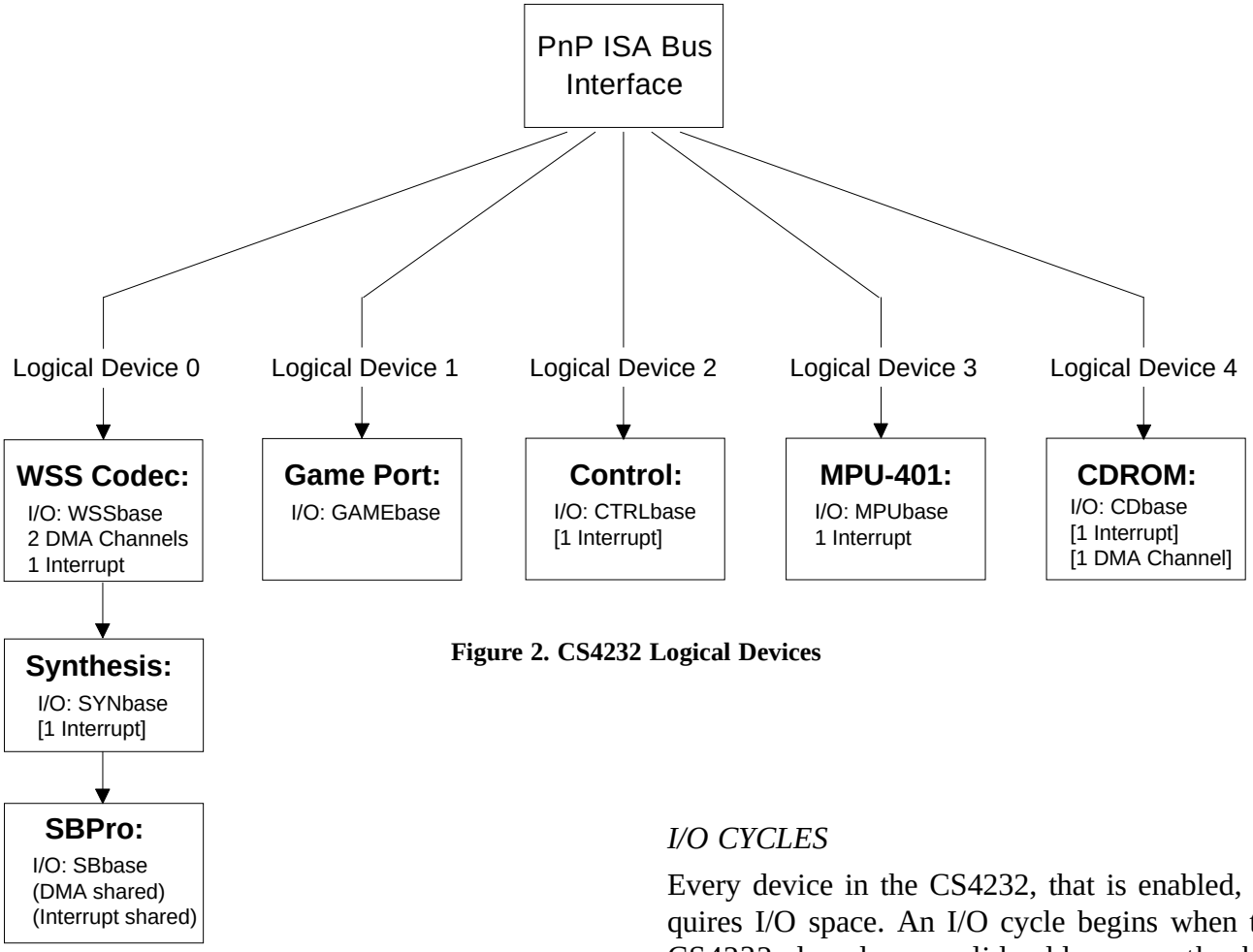


Figure 2. CS4232 Logical Devices

ISA Bus Interface

The 8-bit parallel I/O and 8-bit parallel DMA ports of the CS4232 provide an interface which is compatible with the Industry Standard Architecture (ISA) bus. The ISA Interface enables the host to communicate with the various functional blocks within the CS4232 via two types of accesses: Programmed I/O (PIO) access, and DMA access.

A number of configuration registers must be programmed prior to any accesses by the host computer. The configuration registers are programmed via a Plug and Play configuration sequence or via configuration software provided by Crystal Semiconductor.

I/O CYCLES

Every device in the CS4232, that is enabled, requires I/O space. An I/O cycle begins when the CS4232 decodes a valid address on the bus while the DMA acknowledge signals are inactive and AEN is low. The $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ signals determine the direction of the data transfer. For read cycles, the CS4232 will drive data on the DATA lines while the host asserts the $\overline{\text{IOR}}$ strobe. Write cycles require the host to assert data on the DATA lines and strobe the $\overline{\text{IOW}}$ signal. The CS4232 will latch data on the rising edge of the $\overline{\text{IOW}}$ strobe.

I/O ADDRESS DECODING

The logical devices inside the CS4232 use 10-bit or 12-bit address decoding. The Synthesizer, Sound Blaster, Game Port, MPU-401, and CDROM devices support 10-bit address decoding, while the Windows Sound System and Control devices support 12-bit address decoding. Devices that support 10-bit address decoding, re-

quire A10 and A11 be zero for proper decode; therefore, no aliasing occurs through the 12-bit address space.

To prevent aliasing into the upper address space, the CS4232 supports a "16-bit decode" option, where the upper address bits SA12 through SA15 can be connected to the CS4232. SA12-SA15 are then decoded to be 0,0,0,0 for all logical device address decoding. When the upper address bits are used, the CDROM interface is no longer available since the upper address pins are multiplexed with the CDROM (See *Reset and Power Down* section).

DMA CYCLES

The CS4232 supports up to three 8-bit ISA-compatible DMA channels. The only allowed configuration, which cannot be modified, is:

DMA A = ISA DMA channel 0
DMA B = ISA DMA channel 1
DMA C = ISA DMA channel 3

The typical configuration would require two DMA channels. One for the WSS Codec and Sound Blaster playback, and the other for WSS Codec capture (to support full-duplex). The CDROM, if used, can also support a DMA channel, although this is not typical.

DMA cycles are distinguished from control register cycles by the generation of a DRQ (DMA Request) by the CS4232. The host acknowledges the request by generating a $\overline{\text{DACK}}$ (DMA Acknowledge) signal. The transfer of audio data occurs during the $\overline{\text{DACK}}$ cycle. During the $\overline{\text{DACK}}$ cycle the CS4232 ignores the addresses on the address lines.

The digital audio data interface uses DMA request/grant pins to transfer the digital audio data between the CS4232 and the ISA bus. The CS4232 is responsible for generating a request signal whenever the CS4232's internal buffers require updating. Upon receipt of a DMA request, the host processor responds with an acknowledge signal and a command strobe which transfers data to and from the CS4232, eight bits at a time. The CS4232 holds the request pin active until the appropriate number of 8-bit cycles have occurred. The number of 8-bit transfers will vary depending on the digital audio data format, bit resolution, and operation mode.

The CS4232 may assert the DMA request signal at any time. Once asserted, the DMA request will remain asserted until a complete DMA cycle occurs to the CS4232. A complete DMA cycle consists of one or more bytes depending on which device internal to the CS4232 is generating the request.

INTERRUPTS

The CS4232 supports six interrupt pins for Plug and Play flexibility, although only one or two are typically used. The only allowed hardware connections, which cannot be modified, are:

IRQ A = ISA Interrupt 5
IRQ B = ISA Interrupt 7
IRQ C = ISA Interrupt 9
IRQ D = ISA Interrupt 11
IRQ E = ISA Interrupt 12
IRQ F = ISA Interrupt 15

The typical configuration would support two interrupt sources: one shared between the WSS Codec and the Sound Blaster Pro compatible devices, and the other for the MPU401 device. Interrupts are also supported for the Synthesizer, Control, and CDROM devices, but are typically not used.

PLUG AND PLAY

The Plug and Play (PnP) interface provides the necessary logic to make the CS4232 compatible with the Intel/Microsoft Plug-and-Play specification for an ISA-bus device. Since the CS4232 is an ISA-bus device, it only supports ISA-compatible IRQs and DMA channels. Plug and Play compatibility allows the PC to automatically

configure the CS4232 into the system upon power up. Plug and Play capability optimally resolves conflicts between Plug and Play and non-Plug and Play devices within the system. Alternatively, the PnP feature of the CS4232 can be bypassed. See the *Bypassing PnP* section for more information. The CS4232 PnP interface operates in accordance with the *Plug and Play ISA Specification* published by Intel and Microsoft. For a detailed Plug and Play protocol description, please refer to the latest revision of the *Plug and Play ISA Specification*.

To support Plug and Play in ISA systems that do not have a PnP BIOS or a PnP-aware operating system, the Configuration Manager (CM) TSR and an ISA Configuration Utility (ICU) are used to provide these functions. The CM isolates the cards, assigns Card Select Numbers, reads PnP card resource requirements, and allocates resources to the cards based on system resource availability. The ICU is used to keep the BIOS and the CM informed of the current system configuration. It also aids users in determining configurations for non-PnP ISA cards. A more thorough discussion of the Configuration Manager and the ISA Configuration Utility can be found in the *Product Development Information* document of the Plug and Play Kit by Intel Corp. In a PnP BIOS system, the BIOS is responsible for configuring at least all system board PnP devices. Some systems require additional software to aid the BIOS in configuring PnP ISA cards. The PnP BIOS can execute all PnP functions independently of the type of operating system. However, if a PnP aware operating system is present, the PnP responsibilities are shared between the BIOS and the operating system. For more information regarding PnP BIOS, please refer to the latest revision of the *Plug and Play BIOS Specification* published by Compaq Computer, Phoenix Technologies, and Intel.

The Plug and Play configuration sequence maps the various functional blocks of the CS4232 (logical devices) into the host system address space and configures both the DMA and interrupt channels. The host has access to the CS4232 via three 8-bit auto-configuration ports: Address port (0279h), Write Data port (0A79h), and relocatable Read Data port (0200h - 03FFh). The read data port is relocated automatically by PnP software when a conflict occurs.

The configuration sequence is as follows:

1. Host sends a software key which places all PnP cards in the sleep state (or Plug-and-Play mode).

2. The CS4232 is isolated from the system using an isolation sequence.

3. A unique identifier (handle) is assigned to the CS4232 and the resource data is read.

4. After all cards' resource requirements are determined, the host uses the handle to assign conflict free resources to the CS4232

5. After the configuration registers have been programmed, each configured logical device is activated.

6. The CS4232 is then removed from Plug-and-Play mode.

Upon power-up, the chip is inactive and must be enabled via software. The CS4232 hardware monitors writes to the PnP Auto-Configuration Address port (0279h). If the host sends a PnP initiation key, consisting of a series of 32 predefined byte writes, the hardware will detect the key and place the CS4232 into the Plug-and-Play (PnP) mode. Another method to program the part is to use a special Crystal initiation key which functions like the PnP initiation key, but can be invoked by the user at any time However, the Crystal Key only supports one CS4232 per system. The Crystal key and special commands are detailed in the *Crystal Key* and *Bypassing PnP* sections.

The isolation sequence uses a unique 72-bit serial identifier which is stored in the CS4232. The host performs 72 pairs of I/O read accesses to the Read Data port. The identifier determines what data is put on the data bus in response to those read accesses. When the isolation sequence is complete, the CM assigns a Card Select Number (CSN) to the CS4232. This number distinguishes the CS4232 from the other PnP devices in the system. The CM then reads the resource data from the CS4232. The 72-bit identifier and the resource data is either stored in an external user-programmable E^2PROM, or loaded via a 'hostload" procedure from BIOS before PnP software is initiated.

The CM determines the necessary resource requirements for the system and then programs the CS4232 through the configuration registers. The configuration register data is written one logical device at a time. After all logical devices have been configured, the CM activates each one individually. Each logical device is now available on the ISA bus and will respond to the programmed I/O address range, DMA channels, and interrupts that have been allocated to it.

CS4232 PnP Data

The CS4232 hardware configuration and Plug and Play configuration data must be loaded into the CS4232 RAM. The data may be stored in an external E^2PROM or may be downloaded from the host.

To load the data, refer to the *Loading Resource Data* section. The following is the CS4232 Plug and Play resource data:

The first nine bytes of the PnP resource data are the Plug and Play ID, which uniquely identifies the CS4232 from other PnP devices. The Crystal default is broken down as follows:

0Eh, 63h - Crystal ID - 'CSC' in compressed ASCII. (See the PnP Spec for more information)

42h, 32h - Crystal Product Number

01, 00, 00, 00 - Serial number. This can be modified by each OEM to uniquely identify their card.

D3h - Checksum. Must be recalculated if the serial number is changed.

Crystal software uses the first four bytes to indicate the presence of the CS4232 part; therefore, the first four bytes must not be altered from those listed above.

The next 3 bytes are the PnP version number. The default is version 1.0: 0Ah, 10h, 00h.

The next sequence of bytes are the ANSI identifier string. The default is: 82h, 07h, 00h, 'CS4232', 00h.

The following logical device data must be entered using the PnP ISA Specification format. The actual logical device values are found in Table 1.

Logical Device 0
Dependent Functions - See Table 1
ANSI String = "WSS/OPL/SB"

Logical Device 1
Dependent Functions - See Table 1
ANSI String = "GAME"

Logical Device 2
Dependent Functions - See Table 1
ANSI String = "CTRL"

Logical Device 3
Dependent Functions - See Table 1
ANSI String = "MPU"

Logical Device 4
Dependent Functions - See Table 1
ANSI String = "CD"

Physical Device	Logical Device	Best Choice	Acceptable Choice 1	Sub optimal Choice 1	Sub optimal Choice 2
WSS	**0**	Compatible ID = PNPB007		ANSI ID = WSS/OPL/SB	
16-bit address decode	I/O Length Alignment	534h-534h 4 4	100-FFCh 4 4		
high true edge sensitive	IRQ	5 (SB share)	5,7,9,11,12,15 (SB share)		
8-bit, count by byte, type A	DMA	1 (SB Share)	0, 1, 3 (SB share)		
same	DMA	0, 3	----		
Synthesis	**0**	Compatible ID = PNPB020			
10-bit address decode	I/O Length Alignment	388h 4 4	100-3FCh 4 4		
	IRQ	----	----		
SB Pro	**0**	Compatible ID = PNPB002			
10-bit address decode	I/O Length Alignment	220h 16 16	100-3F0h 16 16		
Game Port	**1**	Compatible ID = PNPB02F		ANSI ID = GAME	
10-bit address decode	I/O Length Alignment	200h 8 8	100-3F8h 8 8		
Control	**2**			ANSI ID = CTRL	
16-bit address decode	I/O Length Alignment	100-FF8h 8 8			
	IRQ	----			
MPU401	**3**	Compatible ID = PNPB006		ANSI ID = MPU	
10-bit address decode	I/O Length Alignment	330h 2 8	100-3FCh 2 8		
	IRQ	9	5,7,9,11,12,15		
CD-ROM	**4**			ANSI ID = CD	
10-bit address decode	I/O Length Alignment	100-3FCh 4 4			
	IRQ	----			
	DMA	----			

---- Feature not supported in the listed configuration, but is supported through customization.

Table 1. Typical Plug and Play Resource Data

Loading Resource Data

The CS4232 provides a serial E^2PROM interface to allow user-programmable serial number and resource data to be stored in an external E^2PROM. The interface is compatible with devices from a number of vendors and the size may vary according to specific customer requirements. The largest configuration supported by the CS4232 internal RAM is 256 bytes of combined hardware configuration and PnP resource data. With the addition of the 4-byte header, the maximum amount of E^2PROM space used would be 260 bytes. After power-up, the CS4232 looks for the existence of an E^2PROM by reading the first two bytes from the E^2PROM interface. If the data from the E^2PROM port reads 55h and AAh, then the rest of the E^2PROM data is loaded into the CS4232 internal RAM. If the first two bytes aren't 55h and AAh, then a "hostload" procedure must be used to load the internal RAM. The Hostload procedure can be found in the *Hostload* section. If the CS4232 is embedded in a motherboard, an external E^2PROM is not necessary, since the BIOS can control the bootup sequence and ensure that a Hostload sequence is performed prior to a PnP sequence. If the CS4232 is installed on a plug-in card, then an external E^2PROM is strongly recommended to ensure that the proper PnP resource data is loaded into the CS4232 internal RAM prior to a PnP sequence. See the *External E^2PROM* section for more information on the serial E^2PROM interface and E^2PROM programming.

The format for the data stored in the E^2PROM is as follows:

(CS4232 Hardware Configuration Data:)
- 2 bytes E^2PROM validation: 55h, AAh
- 2 bytes length of resource data in E^2PROM
- 7 bytes CS4232 hardware configuration

(Plug and Play Resource Data:)
- 9 bytes Plug and Play ID
- 3 bytes Plug and Play version number
- Variable number of bytes of user defined ASCII ID string
- Logical Device 0 (Windows Sound System, OPL3, Sound Blaster Pro) data
- Logical Device 1 (Game Port) data
- Logical Device 2 (Control) data
- Logical Device 3 (MPU-401) data
- Logical Device 4 (CD-ROM) data
- End of Resource byte & checksum byte

A typical E^2PROM data load, in assembly format, can be found in Appendix A.

The Crystal Key

A special Crystal key may be used to place the CS4232 in the configuration mode. Once the Crystal key has been initiated, new PnP default resource data can be downloaded by a hostload sequence, or an alternate method of programming the configuration registers may be used. This alternate method is referred to as the "SLAM" method. The SLAM method allows the user to directly access the configuration registers, configure, and activate the chip, and then, optionally, disable the PnP feature of the

CS4232. The SLAM method uses commands that are similar to the PnP commands; however, they are different since the user has direct access to the configuration registers. To use the SLAM method, see the *Bypassing PnP* section.

The Crystal Key cannot differentiate between multiple CS4232 ICs; therefore, it should only be used in systems that do not plan on supporting multiple CS4232 ICs. To support multiple parts in a Plug-and-Play environment, the Plug-and-Play isolation key should be used, since the PnP 9-byte identifier can distinguish between multiple CS4232 ICs.

The following 32 bytes, in hex, are the Crystal key:

96, 35, 9A, CD, E6, F3, 79, BC,

5E, AF, 57, 2B, 15, 8A, C5, E2

F1, F8, 7C, 3E, 9F, 4F, 27, 13,

09, 84, 42, A1, D0, 68, 34, 1A

Bypassing Plug and Play

The SLAM method allows the user to bypass the Plug and Play features, and, optionally, act like a non-Plug and Play or legacy device; however, the SLAM method only supports one CS4232 IC per system. The user directly programs the resources into the CS4232, and then optionally disables the PnP feature, which forces the CS4232 to disregard any future PnP initiation key sequences (All activated logical devices appear as legacy devices to PnP). The CS4232 will still respond to the Crystal key.

To use the SLAM method, the following sequence must be followed:

1. Host sends 32-byte Crystal key to I/O 0279h, chip enters configuration mode.

2. Host programs CSN (Card Select Number) by writing a 06h and xxh to I/O 0279h.

3. Host programs the configuration registers of each logical device by writing to I/O 0279h. The following data is the maximum amount of information per device. All current devices only need a subset of this data:

   Logical Device ID (15h, xxh)

   I/O Port Base Address 0 (47h, xxh, xxh) high byte , low byte

   I/O Port Base Address 1 (48h, xxh, xxh) high byte , low byte

   I/O Port Base Address 2 (42h, xxh, xxh) high byte , low byte

   Interrupt Select 0 (22h, xxh)

   Interrupt Select 1 (27h, xxh)

   DMA Select 0 (2Ah, xxh)

   DMA Select 1 (25h, xxh)

   Activate Device (33h, 01h)

4. Repeat #3 for each logical device to be enabled. (Not all devices need be enabled.)

5. Host activates chip/card by writing a 79h to I/O 0279h .

6. (Optional) Host disables CS4232 PnP feature by writing a 55h to CTRLbase+5. The CS4232 will not participate in any future PnP cycles.

NOTE: To enable the PnP feature after it has been disabled by the SLAM method, the CS4232 must be reset by bringing RESDRV pin to a logic high or by removing power from the device.

The following illustrates typical data sent to the CS4232 using the SLAM method.

```
006h, 001h          ; CSN=1

015h, 000h          ; LOGICAL DEVICE 0
047h, 005h, 034h    ; WSSbase = 0x534
048h, 003h, 088h    ; SYNbase = 0x388
042h, 002h, 020h    ; SBbase = 0x220
022h, 005h          ; WSS & SB IRQ = 5
02Ah, 001h          ; WSS & SB DMA0 = 1
025h, 003h          ; WSS capture DMA1 = 3
033h, 001h          ; activate logical device 0

015h, 001h          ; LOGICAL DEVICE 1
047h, 002h, 000h    ; GAMEbase = 0x200
033h, 001h          ; activate logical device 1

015h, 002h          ; LOGICAL DEVICE 2
047h, 001h, 020h    ; CTRLbase = 0x120
033h, 001h          ; activate logical device 2

015h, 003h          ; LOGICAL DEVICE 3
047h, 003h, 030h    ; MPUbase=0x330
022h, 009h          ; MPU IRQ = 9
033h, 001h          ; activate logical device 3

079h                ; activate CS4232 part
```

If all the above data is sent to the CS4232, after the Crystal key, all devices except the CDROM will respond to the appropriate resources given.

Hardware Configuration Data

The hardware configuration data, or resource header, contains mapping information that links interrupt and DMA pins with actual interrupt numbers used by PnP and SLAM procedures. In the current silicon, this mapping is fixed and should not be changed. Future products will allow remapping of the hardware. This data also controls the XCTL0/XA2 pin functionality. The hardware configuration data is a resource header on top of the PnP resource data.

The resource header is either seven or eleven bytes long and contains the data necessary to configure the CS4232 hardware. If an E^2PROM is not used (Hostload), the first four bytes are not part of the header, which means the header is only seven bytes long. The resource header maps the many functions of the logical devices to the physical pins of the CS4232 chip. Table 2 contains the CS4232 hardware configuration data.

The first actual byte of hardware resource data is byte 5 in Table 2. This byte determines the function of the XCTL0/XA2 pin. The default of 0, forces the pin to the control function XCTL0, and the external peripheral port supports only 4 I/O locations through XA0-XA1. If this byte is set to 008h, the pin switches to the XA2 function and the peripheral port supports 8 I/O locations through XA0-XA2. When using the hostload procedure, this byte is loaded second, not first.

The next byte, listed as byte 6, will allow future support of mixer mapping. This feature is not currently implemented; therefore, this byte must be 48h for current silicon. When using the hostload procedure, this byte is loaded first, not second.

Bytes 7 through 9 map the interrupt number to the actual interrupt pins A - F. This feature is not currently supported. The default data must not be changed.

Bytes 10 and 11 map the DMA channel number to the actual DMA pins A-C. This feature is not currently supported. The default data must not be changed.

BYTE	Default	Description
1	55h	E^2PROM validation byte 1. The first two bytes tell the CS4232 that the E^2PROM exists.
2	AAh	E^2PROM validation byte 2
3*	00h	High byte for length of resource data in E^2PROM- Reserved, must be 00
4	DDh	Low byte for length of resource data in E^2PROM
5†	00h	External Peripheral Port I/O Decode Address Length 00 = 4 bytes, 08 = 8 bytes 008h causes XCTL0/XA2 pin to change to peripheral port address bit XA2.
6*†	48h	Mixer Mapping B7/6 for LINE, B5/4 for AUX1, B3/2 for AUX2, B1/0 - reserved = 0 Value: 0 - Line In, 1 - FM/SYNTH, 2 - CD, 3 - other
7*	75h	IRQ A/B Selection: Lower nibble = A, Upper nibble = B. Along with next two bytes - specify hardware interrupts tied to CS4232 pins
8*	B9h	IRQ C/D Selection: Lower nibble = C, Upper nibble = D.
9*	FCh	IRQ E/F Selection: Lower nibble = E, Upper nibble = F.
10*	10h	DMA A/B Selection: Lower nibble = A, Upper nibble = B. This byte and the next byte - specify hardware DRQ/DACKs tied to the CS4232 pins
11*	03h	DMA C Selection: Lower nibble = C, Upper nibble = reserved (must be 0).

NOTE:The first four bytes are exclusive to the E^2PROM and are not used in the Hostload mode.
* Currently not supported. Must be set to default values given in the table.
† Byte 5 and 6 must be swapped when loading the CS4232 IC directly - Hostload procedure

Table 2. Hardware Resource Data

Hostload Procedure

To download PnP resource data from the host, as opposed to the E^2PROM, to the CS4232 internal RAM, use the following sequence:

1. Configure Control I/O base address, CTRLbase, by one of two methods: regular PnP cycle or Crystal Key method.

   a. The host can use the regular PnP cycle to program the CTRLbase, and then place the chip in the wait_for_key_state

   b. If the Crystal Key method is used:

      First, send the 32-byte Crystal key to I/O address 0279h. (The Crystal Key only supports one CS4232 IC per system.)

      Second, configure logical device 2 base address, CTRLbase, by writing to I/O 0279h (15h, 02h, 47h, xxh, xxh, 33h, 01h, 79h).
      Note: The two xxh represent the base_address_high and base_address_low respectively. The default is: 01h, 20h.

2. Download the PnP resource data.

   a. Send download command by writing AAh to CTRLbase+5.

   b. Send starting download address (2090h) by writing low byte (90h) first, and then high byte (20h) to CTRLbase+5.

   c. Send the resource data in successive bytes to CTRLbase+5. This includes the hardware configuration header and the PnP resource data. The PnP resource format is described in the *CS4232 PnP Data* section. The resource header should not contain the first four bytes which are only used for

E^2PROM loads. Bytes 5 and 6 in Table 2 must be swapped when using the hostload procedure.

d. End download by writing 00h to CTRLbase+6.

e. If any of the Hardware Configuration Data (first 7 bytes) has changed, 5Ah must be written to CTRLbase+5 to force the CS4232 to internally update this information.

The new PnP data is loaded and CS4232 is ready for the next PnP cycle.

External E^2PROM

The Plug and Play specification defines 32 bits of the 72 bit Serial Identifier as being a user defined serial number. To support this function, an interface to an external serial E^2PROM is provided. The E^2PROM also stores default resource data for PnP, and hardware configuration data specific to the CS4232 IC.

The interface is compatible with devices from a number of vendors, such as Xicor's X24C02. After power-on the CS4232 IC looks for the existence of an E^2PROM device and loads the user defined data. This data is read by the PnP software as part of the 72-bit Serial Identifier during the Plug and Play Isolation sequence.

The maximum resource data supported by the CS4232 is 256 bytes, and a four byte header; therefore, the maximum amount of data storage in E^2PROM would be 260 bytes. If an external E^2PROM exists, it is accessed by the serial interface and is connected to the CS4232 XD0 and XA0 pins. The two-wire interface is controlled by three bits in the Control logical device, Hardware Control Register (CTRLbase+1). The serial data can be written to or read from the E^2PROM by sequentially writing or reading that register. The three register bits, D0, D1, D2 are labeled CLK, DOUT, and DIN/EEN respectively. The DIN/EEN bit, when written to a one, enables the E^2PROM serial interface. When the DIN/EEN bit is written to a zero, the serial interface is disabled. The DIN/EEN bit can also be used to read back data from the E^2PROM. The XD0 pin is a bi-directional open-drain data line supporting DIN and DOUT; therefore, to read the correct data, the DOUT bit must be set to a one prior to performing a read of the register. Otherwise, the data read back from DIN/EEN will be all zeros. The E^2PROM data can then be read from the DIN/EEN bit. The CLK bit timing is controlled by the host software. This is the clock for the E^2PROM. The DOUT bit is used to write/program the data out to the E^2PROM. An external pull-up resistor is required on XD0 because it is an open-drain output. Use the guidelines in the specific E^2PROM data sheet to select the value of the pull-up resistor.

Programming the E^2PROM:

1. Configure Control I/O base address by one of two methods: regular PnP cycle or Crystal Key method.

   a. The host can use the regular PnP cycle to program the logical device 2 I/O base address, and then place the chip in the wait_for_key_state

   b. If the Crystal Key method is used:

      First, write to I/O 0279h, send the 32-byte Crystal key. (The Crystal Key only supports one CS4232 IC per system.)

      Second, configure the Control I/O base address by writing 15h, 02h, 47h, 01h, 20h, 33h, 01h, 79h to 0279h.

2. Refer to the specific data sheet for the E^2PROM you are using for timing requirements and data format. Also, refer to the *Loading Resource Data* section of this data sheet for the E^2PROM resource data format.

3. Send the E^2PROM data in successive bits to CTRLbase+1 (Hardware Control Register) while following the E^2PROM data sheet format.

The E^2PROM now contains the PnP resource data. For this new data to take effect, the CS4232 must be reset, causing the CS4232 to read the E^2PROM during initialization.

WINDOWS SOUND SYSTEM CODEC

The WSS Codec software interface consists of 4 I/O locations starting at the Plug and Play address 'WSSbase', and supports 12-bit address decoding. If the upper address bits, SA12-SA15 are used, they must be 0 to decode a valid address. The WSS Codec also requires one interrupt and one or preferably two DMA channels, one for playback and one for capture. Since the WSS Codec and Sound Blaster device are mutually exclusive, the two devices share the same interrupt and DMA playback channel.

The WSS Codec/Mixer is register compatible with the Microsoft Windows Sound System. Functions include stereo Analog-to-Digital and Digital-to-Analog converters (ADCs and DACs), analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, optional A-Law/μ-Law coding, simultaneous capture and playback (at the same sample rates) and a parallel bus interface. Five analog inputs are provided and three can be multiplexed to the ADC. The line input, two auxiliary inputs and a mono input can be mixed with the output of the DAC with full volume control. Several data modes are supported including 8- and 16-bit linear as well as 8-bit companded, 4-bit ADPCM compressed, and 16-bit big Endian.

Enhanced Functions (MODE 2)

The CS4232's initial state is labeled MODE 1 and forces the CS4232 to appear as a CS4248. Enhanced functionality is provided by a second mode on the CS4232 which forces the CS4232 to appear as a CS4231 super set. To switch from MODE 1 to MODE 2, the MODE2 bit should be set to one in the MODE and ID register (I12). When MODE 2 is selected, the bit IA4 in the Index Address register (R0) will be decoded as a valid index pointer providing 16 additional registers and increased functionality over the CS4248.

To reverse the procedure, clear the MODE2 bit and the CS4232 will resume operation in MODE 1. Except for the Capture Data Format (I28), Capture Base Count (I30/31), and Alternate Feature Status (I24) registers, all other Mode 2 functions retain their values when returning to Mode 1. The CS4232's WSS Codec is backwards compatible with the CS4231 and CS4248.

The additional MODE 2 functions are:

1. Full-Duplex DMA support
2. A programmable timer
3. Mono output with mute control
4. Mono input with mixer volume control
5. ADPCM and Big Endian audio data formats
6. Independent selection of capture and playback audio data formats

FIFOs

The WSS Codec contains 16-sample FIFOs in both the playback and capture digital audio data paths. The FIFOs are transparent and have no programming associated with them.

When playback is enabled, the playback FIFO continually requests data until the FIFO is full, and then makes requests as positions inside the FIFO are emptied, thereby keeping the playback FIFO as full as possible. Thus when the system cannot respond within a sample period, the FIFO

starts to empty, avoiding a momentary loss of audio data. If the FIFO runs out of data, the last valid sample can be continuously output to the DACs (if DACZ in I16 is set) which will eliminate pops from occurring.

When capture is enabled, the capture FIFO tries to continually stay empty by making requests every sample period. Thus when the system cannot respond within a sample period, the capture FIFO starts filling, thereby avoiding a loss of data in the audio data stream.

WSS Codec PIO Register Interface

Four I/O mapped locations are available for accessing the Codec functions and mixer. The control registers allow access to status, audio data, and all indirect registers via the index registers. The $\overline{IOR}$ and $\overline{IOW}$ signals are used to define the read and write cycles respectively. A PIO access to the Codec begins when the host puts an address on to the ISA bus which matches WSSbase and drives AEN low. WSSbase is programmed during a Plug and Play configuration sequence. Once a valid base address has been decoded then the assertion of $\overline{IOR}$ will cause the WSS Codec to drive data on the ISA data bus lines. Write cycles require the host to assert data on the ISA data bus lines and strobe the $\overline{IOW}$ signal. The WSS Codec will latch data into the PIO register on the rising edge of the $\overline{IOW}$ strobe.

The audio data interface typically uses DMA request/grant pins to transfer the digital audio data between the WSS Codec and the bus. The WSS Codec is responsible for asserting a request signal whenever the Codec's internal buffers need updating. The bus responds with an acknowledge signal and strobes data to and from the Codec, 8 bits at a time. The WSS Codec keeps the request pin active until the appropriate number of 8-bit cycles have occurred to transfer one audio sample. Note that different audio data types will require a different number of 8-bit transfers.

DMA Interface

The second type of parallel bus cycle from the WSS Codec is a DMA transfer. DMA cycles are distinguished from PIO register cycles by the assertion of a DRQ, while AEN is inactive, followed by an acknowledgment by the host by the assertion of $\overline{DACK}$. While the acknowledgment is received from the host, the WSS Codec assumes that any cycles occurring are DMA cycles and ignores the addresses on the address lines.

The WSS Codec may assert the DMA request signal at any time. Once asserted, the DMA request will remain asserted until a complete DMA cycle occurs to the CS4232. DMA transfers may be terminated by resetting the PEN and/or CEN bits in the Interface Configuration register (I9), depending on the DMA that is in progress (playback, capture, or both). Termination of DMA transfers may only happen between sample transfers on the bus. If DRQ goes active while resetting PEN and/or CEN, the request must be acknowledged with $\overline{DACK}$ and a final sample transfer completed.

DMA CHANNEL MAPPING

Mapping of the WSS Codec's DRQ and $\overline{DACK}$ onto the ISA bus is accomplished by the Plug and Play configuration registers. If the Plug and Play resource data specifies only one DMA channel for the Codec (or the codec is placed in SDC mode) then both the playback and capture DMA requests should be routed to the same DRQ/$\overline{DACK}$ pair (DMA Channel Select 0). If the Plug and Play resource data specifies two DMA channels for the Codec, then the playback DMA request will be routed to the DMA pair specified by the DMA Channel Select 0 resource data, and the capture DMA requests will be routed to the DMA pair specified by the DMA Channel Select 1 resource data.

DUAL DMA CHANNEL MODE

The WSS Codec supports a single and a dual DMA channel mode. In dual DMA channel mode, playback and capture DMA requests and acknowledges occur on independent DMA channels. In dual DMA mode, SDC should be set to 0. The Playback- and Capture-Enables (PEN, CEN, I9) can be changed without a Mode Change Enable (MCE, R0). This allows for proper full duplex control where applications are independently using playback and capture.

SINGLE DMA CHANNEL (SDC) MODE

When two DMA channels are not available, the SDC mode forces all DMA transfers (capture or playback) to occur on a single DMA channel (playback channel). The trade-off is that the WSS Codec will no longer be able to perform simultaneous DMA capture and playback.

To enable the SDC mode, set the SDC bit in the Interface Configuration register (I9). With the SDC bit asserted, the internal workings of the WSS Codec remain exactly the same as dual mode, except for the manner in which DMA request and acknowledges are handled.

The playback of audio data will occur on the playback channel exactly as dual channel operation; however, the capture audio channel is now diverted to the playback channel. Alternatively stated, the capture DMA request occurs on DMA channel select 0 for the WSS Codec. (In MODE 2, the capture data format is always set in register I28.) If both playback and capture are enabled, the default will be playback. SDC does not have any affect when using PIO accesses.

Sound System Codec Register Interface

The Windows Sound System codec is mapped via four locations. The I/O base address, WSSbase, is determined by the Plug and Play configuration. The WSSbase supports four direct registers, shown in Table 3. The first two direct registers are used to access 32 indirect registers shown in Table 4. The Index Address register (WSSbase+0) points to the indirect register that is accessed through the Indexed Data register (WSSbase+1).

This section describes all the direct and indirect registers for the WSS Codec. Table 5 details a summary of each bit in each register with Tables 6 through 11 illustrating the majority of decoding needed when programming the WSS portion of the CS4232, and are included for reference. Tables 6 through 8 indicate gain settings at internal nodes. When enabled, the WSS Codec default state is defined as MODE 1. MODE 1 is backwards compatible with the CS4248 and only allows access to the first 16 indirect registers. Setting the MODE2 bit in the MODE and ID register (I12) enables MODE 2 which allows access to indirect registers 16 through 31 and enables all the features of the WSS Codec.

DIRECT MAPPED REGISTERS

The first two WSS Codec registers provide indirect accessing to more codec registers via an index register. The other two registers provide status information and allow audio data to be transferred to and from the WSS Codec without using DMA cycles or indexing.

Note that register defaults are listed in binary form with reserved bits marked with 'x' to indicate unknown. To maintain compatibility with future parts, these bits must be written as 0, and must be masked off when the register is read. The current value read for reserved bits is not guaranteed on future revisions.

Address	Reg.	Register Name
WSSbase+0	R0	Index Address register
WSSbase+1	R1	Indexed Data register
WSSbase+2	R2	Status register
WSSbase+3	R3	PIO Data register

Table 3. WSS Codec Direct Register

Index	Register Name
I0	Left ADC Input Control
I1	Right ADC Input Control
I2	Left Aux #1 Input Control
I3	Right Aux #1 Input Control
I4	Left Aux #2 Input Control
I5	Right Aux #2 Input Control
I6	Left DAC Output Control
I7	Right DAC Output Control
I8	Fs & Playback Data Format
I9	Interface Configuration
I10	Pin Control
I11	Error Status and Initialization
I12	MODE and ID (MODE2 bit)
I13	Loopback Control
I14	Playback Upper Base Count
I15	Playback Lower Base Count
I16	Alternate Feature Enable I
I17	Alternate Feature Enable II
I18	Left Line Input Control
I19	Right Line Input Control
I20	Timer Low Byte
I21	Timer High Byte
I22	Alternate Sample Frequency
I23	Alternate Feature Enable III
I24	Alternate Feature Status
I25	Version/Chip ID
I26	Mono Input & Output Control
I27	Left Output Attenuation Control
I28	Capture Data Format
I29	Right Output Attenuation Control
I30	Capture Upper Base Count
I31	Capture Lower Base Count

Table 4. WSS Codec Indirect Registers

Index Address Register

(WSSbase+0, R0)

D7	D6	D5	D4	D3	D2	D1	D0
INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0

IA3-IA0 — Index Address: These bits define the address of the indirect register accessed by the Indexed Data register (R1). These bits are read/write.

IA4 — Allows access to indirect registers 16 - 31. Only available in MODE 2. In MODE 1, this bit is reserved.

TRD — Transfer Request Disable: This bit, when set, causes DMA transfers to cease when the INT bit of the Status Register (R2) is set. Independent for playback and capture interrupts.

0 - Transfers Enabled (playback and capture DRQs occur uninhibited)
1 - Transfers Disabled (playback and capture DRQ only occur if INT bit is 0)

MCE — Mode Change Enable: This bit must be set whenever the current mode of the WSS Codec is changed. The Data Format (I8, I28) and Interface Configuration (I9) registers CANNOT be changed unless this bit is set. The exceptions are CEN and PEN which can be changed "on-the-fly". The DAC output is muted when MCE is set.

INIT — WSS Codec Initialization: This bit is read as 1 when the Codec is in a state in which it cannot respond to parallel interface cycles. This bit is read-only.

Immediately after RESET (and once the WSS Codec has left the INIT state), the state of this register is: 010x0000 (binary - where 'x' indicates unknown).

During initialization and software power down (PM1,0 = 01), this register CANNOT be written and always reads 10000000 (80h)

Indexed Data Register

(WSSbase+1, R1)

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7-ID0 — Indexed Data register: These bits are the indirect register referenced by the Indexed Address register (R0).

During initialization and software power down of the WSS Codec, this register can NOT be written and is always read 10000000 (80h)

Status Register

(WSSbase+2, R2, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT

INT — Interrupt Status: This indicates the status of the internal interrupt logic of the WSS Codec. This bit is cleared by any write of any value to this register. The IEN bit of the Pin Control register (I10) determines whether the state of this bit is reflected on the IRQ pin assigned to the WSS Codec.

Read States

0 - Interrupt inactive
1 - Interrupt active

PRDY — Playback Data Ready. The Playback Data register (R3) is ready for more data. This bit would be used when direct programmed I/O data transfers are desired.

0 - Data still valid. Do not overwrite.
1 - Data stale. Ready for next host data write value.

Direct Registers: WSSbase (R0-R3)

ADDRESS		D7	D6	D5	D4	D3	D2	D1	D0
WSSbase+0	R0	INIT	MCE	TRD	IA4†	IA3	IA2	IA1	IA0
WSSbase+1	R1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
WSSbase+2	R2	CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT
WSSbase+3	R3	CD7/PD7	CD6/PD6	CD5/PD5	CD4/PD4	CD3/PD3	CD2/PD2	CD1/PD1	CD0/PD0

Indirect Registers: (I0-I31)

IA4-IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	LMGE	-	LAG3	LAG2	LAG1	LAG0
1	RSS1	RSS0	RMGE	-	RAG3	RAG2	RAG1	RAG0
2	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2M	-	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LDM	-	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
7	RDM	-	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
8 §	FMT1†	FMT0	C/$\overline{L}$	S/$\overline{M}$	CSF2	CSF1	CSF0	C2SL
9 §	CPIO	PPIO	-	CAL1	CAL0	SDC	CEN	PEN
10	XCTL1	XCTL0	OSM1	OSM0	DEN	DTM†	IEN	-
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	1	MODE2	-	-	ID3	ID2	ID1	ID0
13	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
14 *	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
15 *	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
16 §	OLB	TE	CMCE	PMCE	SF1	SF0	SPE	DACZ
17	TEST	TEST	TEST	TEST	APAR	-	XTALE	HPF
18	LLM	-	-	LLG4	LLG3	LLG2	LLG1	LLG0
19	RLM	-	-	RLG4	RLG3	RLG2	RLG1	RLG0
20	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
21	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
22	SRE	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	CS2
23	-	-	-	-	-	-	-	ACF
24	-	TI	CI	PI	CU	CO	PO	PU
25	V2	V1	V0	-	-	CID2	CID1	CID0
26	MIM	MOM	MBY	-	MIA3	MIA2	MIA1	MIA0
27	LOM	-	-	-	LOA3	LOA2	LOA1	LOA0
28 §	FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	-	-	-	-
29	ROM	-	-	-	ROA3	ROA2	ROA1	ROA0
30	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
31	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

† IA4, FMT1, and DTM bits are only available in MODE 2; therefore, regs. 16-31 are only available in MODE 2.

* When in MODE 1, the playback base registers (upper and lower) are used for both playback and capture.

§ For I8, MCE must be set to modify the lower 4 bits. MCE or PMCE must be set to modify the upper 4 bits.
For I9, MCE must be set to modify the upper 6 bits. PEN and CEN can be changed anytime.
For I16, MCE must be set to modify the serial port bits: SF1, SF0, and SPE.
For I28, MCE or CMCE must be set to modify the upper 4 bits.

Table 5. WSS Codec Register Bit Summery

	bit3	bit2	bit1	bit0	Input Gain (I0,I1)	Output Att. (I27,I29)	Mono In (I26)
0	0	0	0	0	0.0 dB	0.0 dB	0.0 dB
1	0	0	0	1	1.5 dB	-2.0 dB	-3.0 dB
2	0	0	1	0	3.0 dB	-4.0 dB	-6.0 dB
3	0	0	1	1	4.5 dB	-6.0 dB	-9.0 dB
.	.	.	.	.	-	-	.
.	.	.	.	.	-	-	.
.	.	.	.	.	-	-	.
12	1	1	0	0	18.0 dB	-24 dB	-36.0 dB
13	1	1	0	1	19.5 dB	-26 dB	-39.0 dB
14	1	1	1	0	21.0 dB	-28 dB	-42.0 dB
15	1	1	1	1	22.5 dB	-30 dB	-45.0 dB

Table 6. Input Gain, Output Atten., and Mono In Levels

	A5	A4	A3	A2	A1	A0	Level
0	0	0	0	0	0	0	0.0 dB
1	0	0	0	0	0	1	-1.5 dB
2	0	0	0	0	1	0	-3.0 dB
3	0	0	0	0	1	1	-4.5 dB
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
60	1	1	1	1	0	0	-90.0 dB
61	1	1	1	1	0	1	-91.5 dB
62	1	1	1	1	1	0	-93.0 dB
63	1	1	1	1	1	1	-94.5 dB

Table 7. DAC & Loopback Attenuation

	SS1	SS0	ADC Input Multiplexer
0	0	0	Line
1	0	1	Auxiliary 1
2	1	0	Microphone
3	1	1	Line Output Loopback

Table 9. ADC Input Selector

CSF			XTAL1	XTAL2
2	1	0	24.576 MHz	16.9344 MHz
0	0	0	8.0 kHz	5.51 kHz
0	0	1	16.0 kHz	11.025 kHz
0	1	0	27.42 kHz	18.9 kHz
0	1	1	32.0 kHz	22.05 kHz
1	0	0	N/A	37.8 kHz
1	0	1	N/A	44.1 kHz
1	1	0	48.0 kHz	33.075 kHz
1	1	1	9.6 kHz	6.62 kHz

Table 10. Sample Frequencies

	A4	A3	A2	A1	A0	Level
0	0	0	0	0	0	12.0 dB
1	0	0	0	0	1	10.5 dB
2	0	0	0	1	0	9.0 dB
3	0	0	0	1	1	7.5 dB
4	0	0	1	0	0	6.0 dB
5	0	0	1	0	1	4.5 dB
6	0	0	1	1	0	3.0 dB
7	0	0	1	1	1	1.5 dB
8	**0**	**1**	**0**	**0**	**0**	**0.0 dB**
9	0	1	0	0	1	-1.5 dB
10	0	1	0	1	0	-3.0 dB
11	0	1	0	1	1	-4.5 dB
12	0	1	1	0	0	-6.0 dB
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
24	1	1	0	0	0	-24.0 dB
25	1	1	0	0	1	-25.5 dB
26	1	1	0	1	0	-27.0 dB
27	1	1	0	1	1	-28.5 dB
28	1	1	1	0	0	-30.0 dB
29	1	1	1	0	1	-31.5 dB
30	1	1	1	1	0	-33.0 dB
31	1	1	1	1	1	-34.5 dB

Table 8. AUX1, AUX2, & LINE Mixer Gain

FMT1	FMT0	C/$\overline{L}$	Data Format
0	0	0	Linear, 8-bit unsigned
0	0	1	µ-Law, 8-bit companded
0	1	0	Linear, 16-bit two's complement, Little Endian
0	1	1	A-Law, 8-bit companded
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit two's complement, Big Endian

Table 11. WSS Codec Data Format

PL/$\overline{R}$ — Playback Left/Right Sample: This bit indicates whether data needed is for the Left channel or Right channel in all data formats except ADPCM. In ADPCM it indicates whether the first two or last two bytes of a 4-byte set (8 ADPCM samples) are needed.

0 - Right or 3/4 ADPCM byte needed
1 - Left, Mono, or 1/2 ADPCM byte needed

PU/$\overline{L}$ — Playback Upper/Lower Byte: This bit indicates whether the playback data needed is for the upper or lower byte of the channel. In ADPCM it indicates, along with PL/$\overline{R}$, which one of the four ADPCM bytes is needed.

0 - Lower or 1/3 ADPCM byte needed
1 - Upper, any 8-bit format, or 2/4 ADPCM byte needed.

SER — Sample Error: This bit indicates that a sample was not serviced in time and an error has occurred. The bit indicates an overrun for capture and underrun for playback. If both the capture and playback are enabled, the source which set this bit can not be determined. However, the Alternate Feature Status register (I24) can indicate the exact source of the error.

CRDY — Capture Data Ready. The Capture Data register (R3) contains data ready for reading by the host. This bit would be used for direct programmed I/O data transfers.

0 - Data is stale. Do not reread the information.
1 - Data is fresh. Ready for next host data read.

CL/$\overline{R}$ — Capture Left/Right Sample: This bit indicates whether the capture data waiting is for the Left channel or Right channel in all audio data formats except ADPCM. In ADPCM it indicates whether the first two or last two bytes of a 4-byte set (8 ADPCM samples) are waiting.

0 - Right or 3/4 ADPCM byte available
1 - Left, Mono, or 1/2 ADPCM byte available

CU/$\overline{L}$ — Capture Upper/Lower Byte: This bit indicates whether the capture data ready is for the upper or lower byte of the channel. In ADPCM it indicates, along with CL/$\overline{R}$, which one of four ADPCM bytes is available.

0 - Lower or 1/3 ADPCM byte available
1 - Upper, any 8-bit format, or 2/4 ADPCM byte available

Note on PRDY/CRDY: These two bits are designed to be read as one when action is required by the host. For example, when PRDY is set to one, the device is ready for more data; or when the CRDY is set to one, data is available to the host. The definition of the CRDY and PRDY bits are therefore consistent in this regard.

I/O DATA REGISTERS

The PIO Data register is two registers mapped to the same address. Writes to this register sends data to the Playback Data register. Reads from this register will receive data from the Capture Data register.

During initialization and software power down of the WSS Codec, this register CANNOT be written and is always read 10000000 (80h)

Capture I/O Data Register

(WSSbase+3, R3, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0 Capture Data Port. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status register (R2). Once all relevant bytes have been read, the state machine will point to the last byte of the sample until a new sample is received from the ADCs. Once the Status register (R2) is read and a new sample is received from the FIFO, the state machine and Status register (R2) will point to the first byte of the new sample.

During initialization and software power down of the WSS Codec, this register can NOT be written and is always read 10000000 (80h)

Playback I/O Data Register

WSSbase+3, R3, Write Only)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD7-PD0 Playback Data Port. This is the control register where playback data is written during programmed IO data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset after the Status register (R2) is read, and the current sample is sent to the DACs via the FIFOs.

INDIRECT MAPPED REGISTERS

These registers are accessed by placing the appropriate index in the Index Address register (R0) and then accessing the Indexed Data register (R1). A detailed description of each indirect register is given below. All reserved bits should be written zero and may be 0 or 1 when read. Note that indirect registers 16-31 are only available when the MODE2 bit in MODE and ID register (I12) is set.

Left ADC Input Control (I0)

Default = 000x0000

D7	D6	D5	D4	D3	D2	D1	D0
LSS1	LSS0	LMGE	res	LAG3	LAG2	LAG1	LAG0

LAG3-LAG0 Left ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

LMGE Left Mic Gain Enable: This bit enables the 20 dB gain stage of the left mic input signal, LMIC.

LSS1-LSS0 Left ADC Input Source Select. These bits select the input source for the left ADC channel.

0 - Left Line: LLINE
1 - Left Auxiliary 1: LAUX1
2 - Left Microphone: LMIC
3 - Left Line Output Loopback

Right ADC Input Control (I1)

Default = 000x0000

D7	D6	D5	D4	D3	D2	D1	D0
RSS1	RSS0	RMGE	res	RAG3	RAG2	RAG1	RAG0

RAG3-RAG0 Right ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

RMGE Right Mic Gain Enable: This bit enables the 20 dB gain stage of the right mic input signal, RMIC.

RSS1-RSS0 Right ADC Input Select. These bits select the input source for the right ADC channel.

0 - Right Line: RLINE
1 - Right Auxiliary 1: RAUX1
2 - Right Microphone: RMIC
3 - Right Line Out Loopback

Left Auxiliary #1 Input Control (I2)

Default = 1xx01000

D7	D6	D5	D4	D3	D2	D1	D0
LX1M	res	res	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

LX1G4-LX1G0 Left Auxiliary #1, LAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

res Reserved. Must write 0. Could read as 0 or 1.

LX1M Left Auxiliary #1 Mute. When set to 1, the left Auxiliary #1 input, LAUX1, to the mixer, is muted.

Right Auxiliary #1 Input Control (I3)

Default = 1xx01000

D7	D6	D5	D4	D3	D2	D1	D0
RX1M	res	res	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

RX1G4-RX1G0 Right Auxiliary #1, RAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

res Reserved. Must write 0. Could read as 0 or 1.

RX1M Right Auxiliary #1 Mute. When set to 1, the right Auxiliary #1 input, RAUX1, to the mixer, is muted.

Left Auxiliary #2 Input Control (I4)

Default = 1xx01000

D7	D6	D5	D4	D3	D2	D1	D0
LX2M	res	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2G4-LX2G0 Left Auxiliary #2, LAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

res Reserved. Must write 0.

LX2M Left Auxiliary #2 Mute. When set to 1, the left Auxiliary #2 input, LAUX2, to the mixer, is muted.

Right Auxiliary #2 Input Control (I5)

Default = 1xx01000

D7	D6	D5	D4	D3	D2	D1	D0
RX2M	res	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

RX2G4-RX2G0 Right Auxiliary #2, RAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

res Reserved. Must write 0. Could read as 0 or 1.

RX2M Right Auxiliary #2 Mute. When set to 1, the right Auxiliary #2 input, RAUX2, to the mixer, is muted.

Left DAC Output Control (I6)

Default = 1x000000

D7	D6	D5	D4	D3	D2	D1	D0
LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0

LDA5-LDA0 — Left DAC Attenuator. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 7.

res — Reserved. Must write 0. Could read as 0 or 1.

LDM — Left DAC Mute. When set to 1, the left DAC output to the mixer will be muted.

Right DAC Output Control (I7)

Default = 1x000000

D7	D6	D5	D4	D3	D2	D1	D0
RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

RDA5-RDA0 — Right DAC Attenuator. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 7.

res — Reserved. Must write 0. Could read as 0 or 1.

RDM — Right DAC Mute. When set to 1, the right DAC output to the mixer will be muted.

Fs and Playback Data Format (I8)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	CSF2	CSF1	CSF0	C2SL

C2SL — Clock 2 Source Select: This bit selects the clock source used for the audio sample rates for both capture and playback. Note that this bit can be disabled by setting SRE in I22. CAUTION: C2SL can only be changed while MCE (R0) is set.

0 - XTAL1 Typically 24.576 MHz
1 - XTAL2 Typically 16.9344 MHz

CFS2-CFS0 — Clock Frequency Divide Select: These bits select the audio sample frequency for both capture and playback. The actual audio sample frequency depends on which clock source (C2SL) is selected and its frequency. Frequencies listed as N/A are not available because their sample frequency violates the maximum specifications; however, the decodes are available and may be used with crystals that do not violate the sample frequency specifications. Note that these bits can be disabled and controlled by bits in I22. CAUTION: CFS2-CFS0 can only be changed while MCE (R0) is set.

Divide	XTAL1 24.576 MHz	XTAL2 16.9344 MHz
0 - 3072	8.0 kHz	5.51 kHz
1 - 1536	16.0 kHz	11.025 kHz
2 - 896	27.42 kHz	18.9 kHz
3 - 768	32.0 kHz	22.05 kHz
4 - 448	N/A	37.8 kHz
5 - 384	N/A	44.1 kHz
6 - 512	48.0 kHz	33.075 kHz
7 - 2560	9.6 kHz	6.62 kHz

S/$\overline{M}$ — Stereo/Mono Select: This bit determines how the audio data streams are formatted. Selecting stereo will result in alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left channel. In MODE 1, this bit is used for both playback and capture. In MODE 2, this bit is only used for playback, and the capture format is independently selected via I28. MCE (R0) or P$\overline{M}$CE (I16) must be set to modify S/$\overline{M}$. See *Changing Audio Data Formats* section for more details.

0 - Mono
1 - Stereo

C/$\overline{L}$, FMT1, and FMT0 bits set the audio data format as shown below. In MODE 1, FMT1, which is forced low, FMT0, and C/$\overline{L}$ are used for both playback and capture. In MODE 2, these bits are only used for playback, and the capture format is independently selected via register I28. MCE (R0) or PMCE (I16) must be set to modify the lower four bits of this register. See *Changing Audio Data Formats* section for more details.

FMT1† D7	FMT0 D6	C/$\overline{L}$ D5	Audio Data Format
0	0	0	Linear, 8-bit unsigned
0	0	1	μ-Law, 8-bit companded
0	1	0	Linear, 16-bit two's complement, Little Endian
0	1	1	A-Law, 8-bit companded
1	0	0	RESERVED
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit two's complement, Big Endian
1	1	1	RESERVED

† FMT1 is not available in MODE 1 (forced to 0).

Interface Configuration (I9)

Default = 00x01000

D7	D6	D5	D4	D3	D2	D1	D0
CPIO	PPIO	res	CAL1	CAL0	SDC	CEN	PEN

PEN — Playback Enable. This bit enables playback. The WSS Codec will generate a DRQ and respond to DACK signal when this bit is enabled and PPIO=0. If PPIO=1, PEN enables PIO playback mode. PEN may be set and reset without setting the MCE bit.

0 - Playback Disabled (playback DRQ and PIO inactive)
1 - Playback Enabled

CEN — Capture Enabled. This bit enables the capture of data. The WSS Codec will generate a DRQ and respond to DACK signal when CEN is enabled and CPIO=0. If CPIO=1, CEN enables PIO capture mode. CEN may be set and reset without setting the MCE bit.

0 - Capture Disabled (capture DRQ and PIO inactive)
1 - Capture Enabled

SDC — Single DMA Channel: This bit will force BOTH capture and playback DMA requests to occur on the Playback DMA channel. This bit forces the WSS Codec to use one DMA channel. Should both capture and playback be enabled in this mode, only the playback will occur. See the *DMA Interface* section for further explanation.

0 - Dual DMA channel mode
1 - Single DMA channel mode

CAL1,0 — Calibration: These bits determine which type of calibration the WSS Codec performs whenever the Mode Change Enable (MCE) bit, R0, changes from 1 to 0. The number of sample periods required for calibration is listed in parenthesis.

0 - No calibration (0, 40 the first time)
1 - Converter calibration (136)
2 - DAC calibration (40)
3 - Full calibration (168)

PPIO — Playback PIO Enable: This bit determines whether the playback data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

CPIO — Capture PIO Enable: This bit determines whether the capture data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

Caution: This register, except bits CEN and PEN, can only be written while in Mode Change Enable (either MCE or PMCE). See the *Changing Sampling Rate* section for more details..

Pin Control (I10)

Default = 0000000x

D7	D6	D5	D4	D3	D2	D1	D0
XCTL1	XCTL0	OSM1	OSM0	DEN	DTM	IEN	res

res — Reserved. Must write 0. Could read as 0 or 1.

IEN — Interrupt Enable: This bit enables the interrupt pin. The Interrupt pin will reflect the value of the INT bit of the Status register (R2). The interrupt pin is active high.

0 - Interrupt disabled
1 - Interrupt enabled

DTM — DMA Timing Mode. Mode 2 only. When set, causes the current DMA request signal to be deasserted on the rising edge of the IOW or IOR strobe during the next to last byte of a DMA transfer. When DTM = 0 the DMA request is released on the falling edge of the IOW or IOR during the last byte of a DMA transfer.

DEN — Dither Enable: When set, triangular pdf dither is added before truncating the ADC 16-bit value to 8-bit, unsigned data. Dither is only active in the 8-bit unsigned data mode.

0 - Dither enabled
1 - Dither disabled

OSM1-OSM0 — These bits are enabled by setting SRE = 1 in I22. These bits in combination with DIV5-DIV0 and CS2 (I22) determine the current sample rate of the WSS Codec when SRE = 1

00 - 12kHz < Fs ≤ 24kHz
01 - Fs > 24kHz
10 - Fs ≤ 12kHz
11 - reserved

XCTL1-XCTL0 — XCTL Control: These bits are reflected on the XCTL1,0 pins of the CS4232. NOTE: These pins are multiplexed with other functions; therefore, they may not be available on a particular design.

0 - TTL logic low on XCTL1,0 pins
1 - TTL logic high on XCTL1,0 pins

Error Status and Initialization (I11, Read Only)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1-ORL0 — Overrange Left Detect: These bits determine the overrange on the left ADC channel. These bits are updated on a sample by sample basis.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

ORR1-ORR0 — Overrange Right Detect: These bits determine the overrange on the Right ADC channel.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

DRS — DRQ Status: This bit indicates the current status of the DRQs assigned to the WSS Codec.

0 - Capture AND Playback DRQs are presently inactive
1 - Capture OR Playback DRQs are presently active

ACI — Auto-calibrate In-Progress: This bit indicates the state of calibration.

0 - Calibration not in progress
1 - Calibration is in progress

PUR — Playback underrun: This bit is set when playback data has not arrived from the host in time to be played. As a result, if DACZ = 0, the last valid sample will be sent to the DACs. This bit is set when an error occurs and will not clear until the Status register (R2) is read.

COR — Capture overrun: This bit is set when the capture data has not been read by the host before the next sample arrives. The old sample will not be overwritten and the new sample will be ignored. This bit is set when an error condition occurs and will not clear until the Status register (R2) is read.

The SER bit in the Status register (R2) is simply a logical OR of the COR and PUR bits. This enables a polling host CPU to detect an error condition while checking other status bits.

MODE and ID (I12)

Default = 10xx1010

D7	D6	D5	D4	D3	D2	D1	D0
1	MODE2	res	res	ID3	ID2	ID1	ID0

ID3-ID0 — Codec ID: These four bits indicate the ID and initial revisions of the codec. Further revisions are expanded in indirect register 25. These bits are read only.

0001 - Rev B CS4248/CS4231
1010 - Rev C CS4248/CS4231 and all CS4232s. See register 25

res — Reserved. Must write 0. Could read as 0 or 1.

MODE2 — MODE 2: Enables the expanded mode of the CS4232. Must be set to enable access to indirect registers 16-31 and their associated features.

0 - MODE 1: CS4248 "look-alike".
1 - MODE 2: Expanded features.

Loopback Control (I13)

Default = 000000x0

D7	D6	D5	D4	D3	D2	D1	D0
LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	res	LBE

LBE — Loopback Enable: When set to 1, the ADC data is digitally mixed with data sent to the DACs.

0 - Loopback disabled
1 - Loopback enabled

res — Reserved. Must write 0. Could read as 0 or 1.

LBA5-LBA0 — Loopback Attenuation: These bits determine the attenuation of the loopback from ADC to DAC. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 7.

Playback Upper Base (I14)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0

PUB7-PUB0 — Playback Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. The Current Count registers cannot be read. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

Playback Lower Base (I15)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0

PLB7-PLB0 — Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

Alternate Feature Enable I (I16)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
OLB	TE	CMCE	PMCE	SF1	SF0	SPE	DACZ

DACZ — DAC Zero: This bit will force the output of the playback channel to AC zero when an underrun error occurs

1 - Go to center scale
0 - Hold previous valid sample

SPE — Serial Port Enable. When enabled, audio data from the ADCs is sent out SDOUT and audio data from SDIN is sent to the DACs.

1 - Enable serial port
0 - Disable serial port. ISA Bus used for audio data.

SF1,SF0 — Serial Format. Selects the format of the serial port when enabled by SPE.

0 - 64-bit enhanced. Figure 6.
1 - 64-bit. Figure 7.
2 - 32-bit. Figure 8.
3 - Reserved

PMCE — Playback Mode Change Enable. When set, it allows modification of the stereo/mono and audio data format bits (D7-D4) for the playback channel, I8. MCE in R0 must be used to change the sample frequency.

CMCE — Capture Mode Change Enable. When set, it allows modification of the stereo/mono and audio data format bits (D7-D4) for the capture channel, I28. MCE in R0 must be used to change the sample frequency in I8.

TE — Timer Enable: This bit, when set, will enable the timer to run and interrupt the host at the specified frequency in the timer registers.

OLB — Output Level Bit: Provided for backwards compatibility. OLB on the CS4232 is always set internally providing a typical output full-scale voltage of 2.8 Vpp.

Alternate Feature Enable II (I17)

Default = 0000x000

D7	D6	D5	D4	D3	D2	D1	D0
TEST	TEST	TEST	TEST	APAR	res	XTALE	HPF

HPF — High Pass Filter: This bit enables a DC-blocking high-pass filter in the digital filter of the ADC. This filter forces the ADC offset to 0.

0 - disabled
1 - enabled

XTALE — Crystal Enable. Provided for backwards compatibility with the CS4231A. Both crystals are always active on the CS4232.

res — Reserved. Must write 0. Could read as 0 or 1.

APAR — ADPCM Playback Accumulator Reset. While set, the Playback ADPCM accumulator is held at zero. Used when pausing a playback stream.

TEST — Factory Test. These bits are used for factory testing and must remain at 0 for normal operation.

Left Line Input Control (I18)

Default = 1xx01000

D7	D6	D5	D4	D3	D2	D1	D0
LLM	res	res	LLG4	LLG3	LLG2	LLG1	LLG0

LLG4-LLG0 — Left Line, LLINE, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

res — Reserved. Must write 0. Could read as 0 or 1.

LLM — Left Line Mute. When set to 1, the left Line input, LLINE, to the mixer, is muted.

Right Line Input Control (I19)

Default = 1xx01000

D7	D6	D5	D4	D3	D2	D1	D0
RLM	res	res	RLG4	RLG3	RLG2	RLG1	RLG0

RLG4-RLG0 — Right Line, RLINE, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 8.

res — Reserved. Must write 0. Could read as 0 or 1.

RLM — Right Line Mute. When set to 1, the Right Line input, RLINE, to the mixer, is muted.

Timer Lower Base (I20)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0

TL7-TL0 — Lower Timer Bits: This is the low order byte of the 16-bit timer base register. Writes to this register cause both timer base registers to be loaded into the internal timer; therefore, the upper timer register should be loaded before the lower. Once the count reaches zero, an interrupt is generated, if enabled, and the timer is automatically reloaded with these base registers.

Timer Upper Base (I21)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0

TU7-TU0 — Upper Timer Bits: This is the high order byte of the 16-bit timer. The time base is determined by the clock source selected from either C2SL in I8 or CS2 in I22.

C2SL = 0 - divide XTAL1 by 245 (24.576 MHz - 9.969 µs)

C2SL = 1 - divide XTAL2 by 168 (16.9344 MHz - 9.92 µs)

Alternate Sample Frequency Select (I22)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
SRE	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	CS2

CS2 — Crystal 2 Select. This bit selects the clock source used for generating the audio sample rate.
0 - XTAL1 = 24.576 MHz
1 - XTAL2 = 16.9344 MHz

DIV5 - DIV0 — Clock Divider. These bits select the audio sample frequency for both capture and playback.

Fs = (2*XTAL)/(M*N)

XTAL = 24.576 MHz CS2 = 0
XTAL = 16.9344 MHz CS2 = 1

N = DIV5-DIV0
$16 \le N \le 49$ for XTAL = 24.576 MHz
$12 \le N \le 33$ for XTAL = 16.9344 MHz

(M set by OSM1,0 in I10)
M = 64 for Fs > 24 kHz
M = 128 for 12 kHz < Fs ≤ 24 kHz
M = 256 for Fs ≤ 12 kHz

SRE — Alternate Sample Rate Enable. When this bit is set to a one, bits 0-3 of I8 will be ignored, and the sample frequency is then determined by CS2, DIV5-DIV0, and the oversampling mode bits OSM1, OSM0 in I10.

Alternate Feature Enable III (I23)

Default = xxxxxxx0

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	ACF

ACF — ADPCM Capture Freeze. When set, the capture ADPCM accumulator and step size are frozen. This bit must be set to zero for adaptation to continue. This bit is used when pausing a ADPCM capture stream.

res — Reserved. Must write 0. Could read as 0 or 1.

Alternate Feature Status (I24)

Default = x0000000

D7	D6	D5	D4	D3	D2	D1	D0
res	TI	CI	PI	CU	CO	PO	PU

PU — Playback Underrun: This bit, when set, indicates that the DAC has run out of data and a sample has been missed.

PO — Playback Overrun: This bit, when set, indicates that the host attempted to write data into a full FIFO and the data was discarded.

CO — Capture Overrun: This bit, when set, indicates that the ADC had a sample to load into the FIFO but the FIFO was full. In this case, this bit is set and the new sample is discarded.

CU — Capture Underrun: This bit indicates that the host has read more data out of the FIFO than it contained. In this condition, the bit is set and the last valid byte is read by the host.

PI — Playback Interrupt: This bit indicates that an interrupt is pending from the playback DMA count registers.

CI — Capture Interrupt: This bit indicates that an interrupt is pending from the capture DMA count registers.

TI — Timer Interrupt: This bit indicates that an interrupt is pending from the timer count registers

res — Reserved. Must write 0. Could read as 0 or 1.

The PI, CI, and TI bits are reset by writing a "0" to the particular interrupt bit or by writing any value to the Status register (R2).

Version / ID (I25)

Default = 101xx010

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	res	res	CID2	CID1	CID0

V2-V0 — Version number. As enhancements are made to the CS4232, the version number is changed so software can distinguish between the different versions.

100 - non-released older version.
101 - 1st version, "C", of CS4232.
These bits are only changed if software features are added. Therefore, future revisions; "D", etc., could have the same version number.

res — Reserved. Must write 0. Could read as 0 or 1.

CID2-CID0 — Chip Identification. Distinguishes between this chip and other codec chips that support this register set.

010 - CS4232. This Data Sheet.
000 - CS4231 or CS4231A

Mono Input and Output Control (I26)

Default = 101x0000

D7	D6	D5	D4	D3	D2	D1	D0
MIM	MOM	MBY	res	MIA3	MIA2	MIA1	MIA0

MIA3-MIA0 — Mono Input Attenuation. When MIM is 0, these bits set the level of MIN summed into the mixer. MIA0 is the least significant bit and represents 3 dB attenuation, with 0000 = 0 dB. See Table 6.

res — Reserved. Must write 0. Could read as 0 or 1.

MBY — Mono Bypass. MBY connects MIN directly to MOUT with an attenuation of 9 dB. When MBY = 1, MIM should be 1.

0 - MIN not connected directly to MOUT.
1 - MIN connected directly to MOUT.

MOM — Mono Output Mute. The MOM bit will mute the mono mix output, MOUT. This mute is independent of the line output mute.

0 - no mute
1 - mute

MIM — Mono Input Mute. Controls the mute function on the mono input, MIN. The mono input provides mix for the "beeper" function in most personal computers. When MIM = 0, MBY should by 0.

0 - no mute
1 - muted

Left Output Attenuation (I27)

Default = 0xxx0000

D7	D6	D5	D4	D3	D2	D1	D0
LOM	res	res	res	LOA3	LOA2	LOA1	LOA0

LOA3-LOA0 — Left Output Attenuation. LOA0 is the least significant bit and represents -2 dB attenuation, with 0000=0dB. See Table 6.

res — Reserved. Must write 0. Could read as 0 or 1.

LOM — Left Output Mute. The LOM bit will mute the left output.

0 - no mute
1 - mute

Capture Data Format (I28)

Default = 0000xxxx

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

S/$\overline{M}$ — Stereo/Mono Select: This bit determines how the capture audio data stream is formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Selecting mono only captures data from the left audio channel. MCE (R0) or C$\overline{M}$CE (I16) must be set to modify S/$\overline{M}$. See *Changing Audio Data Formats* section for more details.

0 - Mono
1 - Stereo

C/L, FMT1, FMT0 set the capture data format in MODE 2. See Table 11 or register I8 for the bit settings and data formats. The capture data format can be different than the playback data format; however, the sample frequency must be the same and is set in I8. MCE (R0) or CMCE (I16) must be set to modify this register. See *Changing Audio Data Formats* section for more details.

Right Output Attenuation (I29)

Default = 0xxx0000

D7	D6	D5	D4	D3	D2	D1	D0
ROM	res	res	res	ROA3	ROA2	ROA1	ROA0

ROA3-ROA0 — Right Output Attenuation. ROA0 is the least significant bit and represents -2 dB attenuation, with 0000 = 0dB. See Table 6.

res — Reserved. Must write 0. Could read as 0 or 1.

ROM — Right Output Mute. The ROM bit will mute the right output.

0 - no mute
1 - mute

Capture Upper Base (I30)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0

CUB7-CUB0 — Capture Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Capture Base register. Reads from this this register returns the same value that was written.

Capture Lower Base (I31)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

CLB7-CLB0 — Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Capture Base register. Reads from this register returns the same value which was written.

SOUND BLASTER INTERFACE

The Sound Blaster Pro compatible interface is the third physical device in logical device 0. Since the WSS Codec and the Sound Blaster are mutually exclusive, the WSS Codec interrupt and playback DMA channel are shared with the Sound Blaster interface. To map volume controls properly, the external devices: FM synthesizer, CDROM, etc., must be connected to the proper analog inputs as illustrated in Figure 3.

Mode Switching

To facilitate switching between different functional modes (i.e. Sound Blaster and Windows Sound System), logic is included in the CS4232 to handle the switch transparently to the host. No special software is required on the host side to perform the mode switch.

Sound Blaster Register Interface

The CS4232's Sound Blaster software interface utilizes 10-bit address decoding and is compatible with Sound Blaster and Sound Blaster Pro interfaces. 10-bit addressing requires that the upper address bits be 0 to decode a valid address, i.e. no aliasing occurs. This device requires 16 I/O locations located at the PnP address 'SBbase'. The following registers, shown in Table 12 are provided for Sound Blaster compatibility.

Left/Right FM Registers,
SBbase+0 - SBbase+3
These registers are mapped directly to the appropriate FM synthesizer registers on the external peripheral port.

Mixer Address Register,
SBbase+4, write only
This register is used to specify the index address for the mixer. This register must be written before any data is accessed from the mixer registers. The mixer indirect register map is shown in Table 13.

Mixer Data Port,
SBbase+5
This port provides read/write access to a particular mixer register depending on the index address specified in the Mixer Address Register.

Address	Description	Type
SBbase+0	Left FM Status Port	Read
SBbase+0	Left FM Register Status Port	Write
SBbase+1	Left FM Data Port	Write Only
SBbase+2	Right FM Status Port	Read
SBbase+2	Right FM Register Status Port	Write
SBbase+3	Right FM Status Port	Write Only
SBbase+4	Mixer Register Address	Write Only
SBbase+5	Mixer Data Port	Read/Write
SBbase+6	Reset	Write Only
SBbase+8	FM Status Port	Read Only
SBbase+8	FM Register port	Write
SBbase+9	FM Data Port	Write Only
SBbase+A	Read Data Port	Read Only
SBbase+C	Command/Write Data	Write
SBbase+C	Write Buffer Status (Bit 7)	Read
SBbase+E	Data Available Status (Bit 7)	Read

Table 12. Sound Blaster Pro Compatible I/O Interface

Reset
SBbase+6, write only
When bit D[0] of this register is set to a one and then set to a zero a reset of the Sound Blaster interface will occur.

Read Data Port
SBbase+A, read only
When bit D[7] of the Data Available Register, SBbase+E, is set =1 then valid data is available in this register. The data may be the result of a Command that was previously written to the Command/Write Data Register or digital audio data.

Command/Write Data
SBbase+C, write only
The Command/Write Data register is used to send Sound Blaster commands to the SBPro interface.

Write Buffer Status,
SBbase+C, read only
The Write Buffer Status register bit D[7] indicates when the SBPro interface is ready to accept another command to the Command/Write Data register. D[7]=1 indicates ready. D[7]=0 indicates not ready.

SOUND BLASTER MIXER REGISTERS

The Sound Blaster mixer registers, shown in Table 13 are shadowed and mapped into the WSS Codec mixer register set. The Sound Blaster mixer to WSS Codec mixer mapping is shown in Figure 3.

Reset Register,
Mixer Index 00H
Writing any value to this register will reset the mixer to default values.

Voice Volume Register,
Mixer Index 04H, Default = 99H
This register provides 8 steps of voice volume control each for the right and left channels.

Microphone Mixing Register,
Mixer Index 0AH, Default = 01H
This register provides 4 steps of microphone mix control.

Input Control Register,
Mixer Index 0CH
This register selects the input source to the ADC.

D2,D1 - 00 - Microphone
01 - CD Audio
10 - Microphone
11 - Line In

Output Control Register,
Mixer Index 0EH

VSTC - 0 - Mono Mode
1 - Stereo Mode

Master Volume Register,
Mixer Index 22H, Default 99H
This register provides 8 steps of master volume control each for the right and left channels.

FM Volume Register,
Mixer Index 26H, Default = 99H
This register provides 8 steps of FM volume control each for the right and left channels.

CD Volume Register,
Mixer Index 28H, Default 01H
This register provides 8 steps of CD volume control each for the right and left channels.

Line-In Volume Register,
Mixer Index 2EH, Default = 01H
This register provides 8 steps of line-in volume control each for the right and left channels.

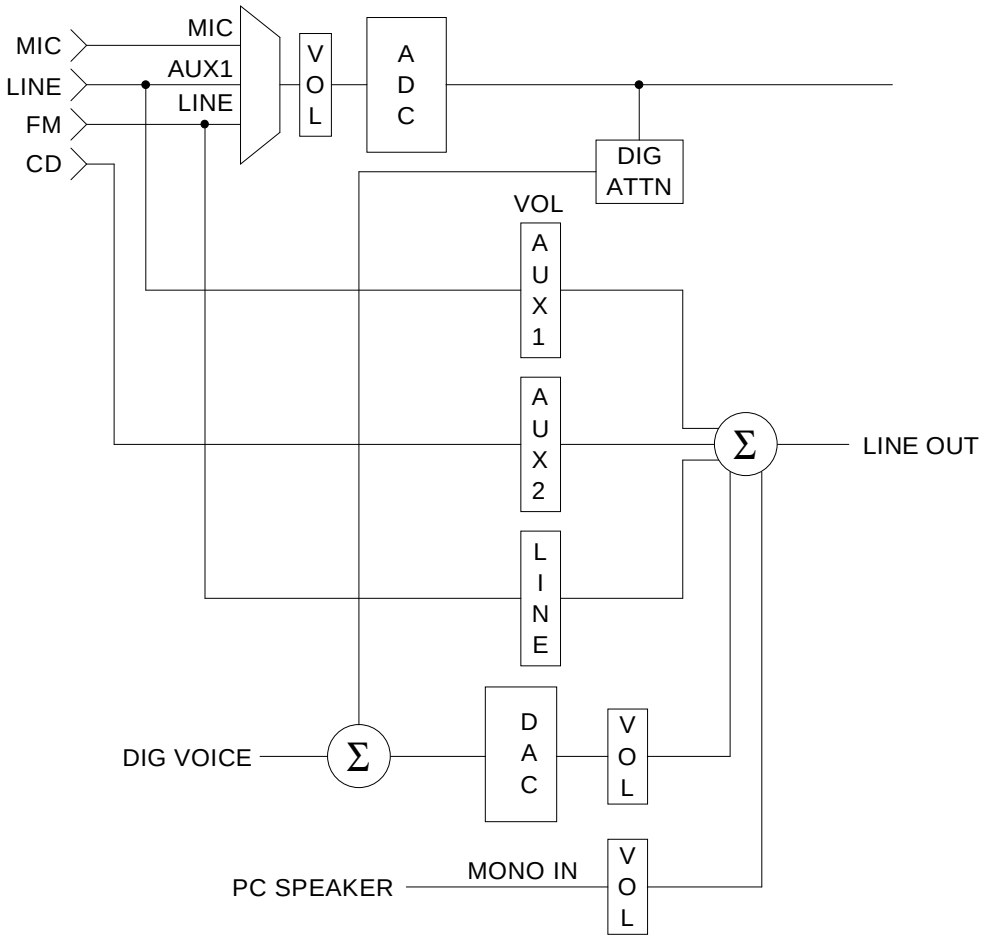


Figure 3. SBPro Mixer Mapping

Register	D7	D6	D5	D4	D3	D2	D1	D0
00H	DATA RESET							
02H	RESERVED							
04H	VOICE VOLUME LEFT				VOICE VOLUME RIGHT			
06H	RESERVED							
08H	RESERVED							
0AH	X	X	X	X	X	MIC MIXING		
0CH	X	X	X			INPUT SELECT		X
0EH	X	X	X	X	X	X	VSTC	X
20H	RESERVED							
22H	MASTER VOLUME LEFT				MASTER VOLUME RIGHT			
24H	RESERVED							
26H	FM VOLUME LEFT				FM VOLUME RIGHT			
28H	CD VOLUME LEFT				CD VOLUME RIGHT			
2AH	RESERVED							
2CH	RESERVED							
2EH	LINE VOLUME LEFT				LINE VOLUME RIGHT			

Table 13. SBPro Compatible Mixer Interface

GAME PORT INTERFACE

The Game Port logical device software interface utilizes 10-bit address decoding and is located at PnP address 'GAMEbase'. 10-bit addressing requires that the upper address bits be 0 to decode a valid address, i.e. no aliasing occurs. For backwards compatibility, the Game Port consists of 8 I/O locations that all alias to the same location, which consists of one read and one write register.

Plug and Play configuration capability will allow the joystick I/O base address, GAMEbase, to be located anywhere within the host I/O address space. Currently most games software assume that the joystick I/O port is located at 200h.

A write to the GAMEbase register triggers four timers. A read from the same register returns four status bits corresponding to the joystick fire buttons and four bits that correspond to the output from the four timers. Each timer output remains low for a period of time determined by the current joystick position.

GAMEbase+0 - GAMEbase+7

D7	D6	D5	D4	D3	D2	D1	D0
JBB2	JBB1	JAB2	JAB1	JBCY	JBCX	JACY	JACX

JACX Joystick A, Coordinate X

JACY Joystick A, Coordinate Y

JBCX Joystick B, Coordinate X

JBCY Joystick B, Coordinate Y

JAB1 Joystick A, Button 1

JAB2 Joystick A, Button 2

JBB1 Joystick B, Button 1

JBB2 Joystick B, Button 2

Two bits are located in the Control register space (CTRLbase+0) for defining the speed of the Game Port Interface. Four different rates are software selectable for use with various joysticks and to support older software timing loops with aliasing (roll-over) problems.

The Game Port hardware interface consists of 8 pins that connect directly to the standard game port connector. For a detailed hardware description, see the *CRD4232-1 Reference Design* Data Sheet.

CONTROL INTERFACE

The Control logical device includes registers for controlling various functions of the CS4232 that are not included in the other logical device blocks. These functions include game port rate control and programmable power management, as well as extra mixing functions.

Control Register Interface

The Control logical device software interface occupies 8 I/O locations, utilizes 12-bit address decoding, and is located at PnP address 'CTRLbase'. If the upper address bits, SA12-SA15 are used, they must be 0 to decode a valid address. This device can also support an interrupt. Table 14 lists the eight Control registers.

Address	**Register**
CTRLbase+0	Joystick & Power Control
CTRLbase+1	E^2PROM Interface & Mixer
CTRLbase+2	Reserved
CTRLbase+3	Reserved
CTRLbase+4	Reserved
CTRLbase+5	Control/Ram Access
CTRLbase+6	Ram Access End
CTRLbase+7	Reserved

Table 14. Control Logical Device Registers

Joystick and Power Control
CTRLbase + 0, Default = 000xxx00

D7	D6	D5	D4	D3	D2	D1	D0
PM1	PM0	CONSW	res	PDP	res	JR1	JR0

JR1,0 — Joystick rate control. Selects operating speed of the joystick.

00 - slowest speed
01 - medium slow speed
10 - medium fast speed
11 - fastest speed

res — Reserved. Must write 0. Could read as 0 or 1.

PDP* — Power Down Processor. When set, places the internal processor in an idle state. This effects the PnP interface, MPU401, and SBPro devices.

CONSW — controls host interrupt generation when a context switch occurs

0 - no interrupt on context switch
1 - Control interrupt generated on context switch

PM1,0 — Power Management. The bits allow different sections of the CS4232 IC to power down while still retaining the PnP data and interface.

00 - All functions active. Typ. 102mA.
01 - A/D and D/A powered down. Mixer still active. Typ. 74mA.
10 - Reserved
11* - WSS Codec, SBPro, MPU401, and PnP interfaces, and the analog mixer are powered down. Typically 30mA.

* NOTE: The SBPro, PnP, and MPU401 interfaces are linked together. Setting PM1,0 or PDP will power all three interfaces down; however, if any one of the interfaces is written to, they will all power back up automatically. PM1,0 and PDP always reflects the value written, not whether the three devices are powered up or not.

E^2PROM Interface & Mixer
CTRLbase+1, Default = xx00x000

D7	D6	D5	D4	D3	D2	D1	D0
res	res	ADC1	ADC0	res	DIN/ EEN	DOUT	CLK

CLK — This bit is used to generate the clock for the Plug and Play E^2PROM. EEN must be set to 1 to make this bit operational.

DOUT — This bit is used to output serial data to the Plug and Play E^2PROM. EEN must be set to 1 to make this bit operational.

DIN/EEN — When read (DIN), this bit reflects the XD0 pin, which should be serial data output from the Plug and Play E^{2}PROM. EEN and DOUT must be 1 for this bit to function.

When written (EEN), enables the E^{2}PROM interface: CLK and DOUT onto the CS4232 peripheral port pins. Writing:

0 - E^{2}PROM interface disabled
1 - E^{2}PROM interface enabled

ADC1,0 — These two bits are used to control an additional A/D mux and enable for an analog loopback path. These two mixing paths provide Karaoke support on the CS4232. See Figure 4.

00 - Normal. A/D input from the input mux.
01 - Codec Input mux is mixed into output mixer. A/D input is from the input mux. This facilitates the Mic mixed to output, but only Mic recorded.
10 - Codec Input mux is mixed into output mixer. A/D input is from line outputs. This facilitates the Mic mixed to output, and the output recorded by the ADCs.
11 - reserved.

res — Reserved. Must write 0. Could read as 0 or 1.

Reserved

CTRLbase+2, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Could read as 0 or 1.

Reserved

CTRLbase+3, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Could read as 0 or 1.

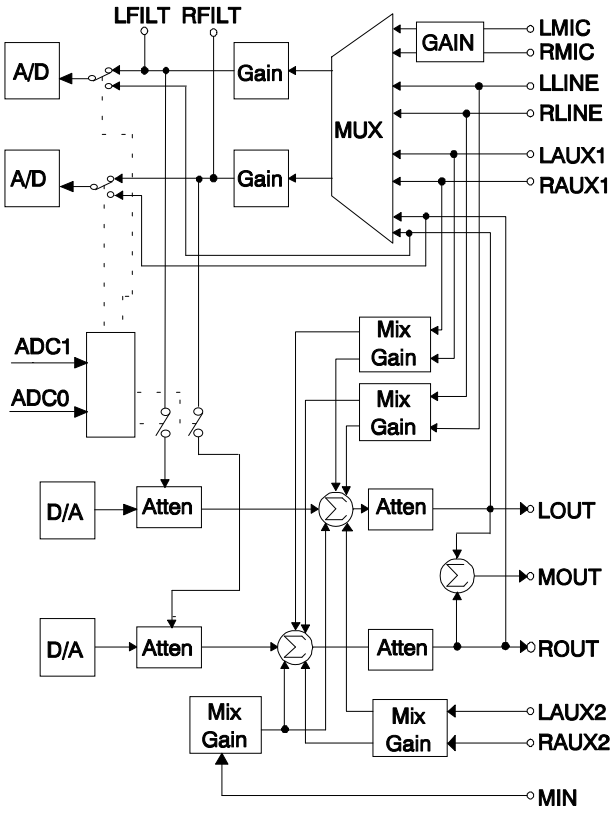


Figure 4. Mixer Addition

Reserved

CTRLbase+4, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Could read as 0 or 1.

Control/RAM Access

CTRLbase+5, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

CR7-CR0 — This register controls the loading of CS4232 internal RAM. RAM support includes hardware configuration and PnP default resource data, as well as program memory. See the *Host-load Procedure* section for more information. Commands are followed by address and data.

RAM Access End

CTRLbase+6, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

RE7-RE0 — A 00 written to this location resets the previous location, CTRLbase+5, from data download to command mode.

Reserved

CTRLbase+7, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Could read as 0 or 1.

MPU-401 INTERFACE

The MPU-401 is an intelligent MIDI interface that was introduced by Roland in 1984. Voyetra Technologies subsequently introduced an IBM-PC plug in card that incorporated the MPU-401 functionality. The MPU-401 has become the de-facto standard for controlling MIDI devices via IBM-PC compatible personal computers.

Although the MPU-401 does have some intelligence, a non-intelligent mode is available in which the MPU-401 operates as a basic UART.

By incorporating hardware to emulate the MPU-401 in UART mode, the CS4232 provides users with MIDI capability.

MPU-401 Register Interface

The MPU401 logical device software interface occupies 2 I/O locations, utilizes 10-bit address decoding, and is located at PnP address 'MPUbase'. 10-bit addressing requires that the upper address bits be 0 to decode a valid address, i.e. no aliasing occurs. The standard base address is 330h. This device also requires an interrupt, typically 9.

MPUbase+0 is the MIDI Transmit/Receive port and MPUbase+1 is the Command/Status port. In addition to I/O decodes the only additional functionality required from an ISA bus viewpoint is the generation of a hardware interrupt whenever data has been received into the receive buffer.

MIDI Transmit/Receive Port,
MPUbase+0, default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0

TR7-TR0 — The MIDI Transmit/Receive Port is used to send and receive MIDI data as well as status information that was returned from a previously sent command.

All MIDI transmit data is transferred through a 64-byte FIFO and receive data through a 16-byte FIFO. The FIFO gives the ISA interface time to respond to the asynchronous MIDI transfer rate of 31.25K baud.

The Command/Status Registers occupy the same address and are used to send instructions to and receive status information from the MPU-401.

Command Register, write only
MPUbase+1

D7	D6	D5	D4	D3	D2	D1	D0
CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

CS7-CS0 — Each write to the Command/Status Register must be monitored and the appropriate acknowledge generated.

Status Register, read only
MPUbase+1, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RXS	TXS	CS5	CS4	CS3	CS2	CS1	CS0

CS5-CS1 — D0-D5 are the 6 LSBs of the last command written to this port.

TXS Transmit Buffer Status Flag.

0 - Transmit buffer not full
1 - Transmit buffer full

RXS Receive Buffer Status Flag

0 - Data in Receive buffer
1 - Receive buffer empty

When in "UART" mode, data is received into the receive buffer FIFO and a hardware interrupt is generated. Data is can be received from two sources: MIDI data via the UART serial input or acknowledge data that is the result of a write to the Command Register (MPUbase+1). The interrupt is cleared by a read of the MIDI Receive Port (MPUbase+0).

MIDI UART

The UART is used to convert parallel data to the serial data required by MIDI. The serial data rate is fixed at 31.25K baud (±1%). The serial data format is RS-232 like: 1 start bit, 8 data bits, and 1 stop bit.

The UART to MIDI external interface should be comprised of a TTL buffer on the transmit line and an off chip OPTO-ISOLATOR on the receive line. In multimedia systems, the MIDI pins are typically connected to the joystick connector. See the *CRD4232-1 Reference Design* Data Sheet for detailed information.

MPU-401 "UART" Mode Operation

After power-up reset, the interface is in "non-UART" mode. Non-UART mode operation is defined as follows:

1. All writes to the Transmit Port, MPUbase+0, are ignored.

2. All reads of the Receive Port, MPUbase+0, return the last received buffer data.

3. All writes to the Command Port, MPUbase+1, are monitored and acknowledged as follows:
   a. A write of 3Fh sets the interface into UART operating mode. An acknowledge is generated by putting an FEh into the receive buffer FIFO which generates an interrupt.

   b. A write of A0-A7, ABh, ACh, ADh, AFh places an FEh into the receive buffer FIFO (which generates an interrupt) followed by a one byte write to the receive buffer FIFO of 00h for A0-A7, and ABh commands, 15h for ACh, 01h for ADh, and 64h for AFh commands.

   c. All other writes to the Command Port are ignored and an acknowledge is generated by putting an FEh into the receive buffer FIFO which generates an interrupt.

UART mode operation is defined as follows:

1. All writes to the Transmit Port, MPUbase+0, are placed in the transmit buffer FIFO. Whenever the transmit buffer FIFO is not empty, the next byte is read from the buffer and sent out the MIDOUT pin. The Status Register, MPUbase+1, bit 6, TXS is updated to reflect the transmit buffer FIFO status.

2. All reads of the Receive Port, MPUbase+0, return the next byte in the receive buffer FIFO. When serial data is received from the MIDIN pin, it is placed in the next receive buffer FIFO location. If the buffer is full, the last location is overwritten with the new data. The Status Register, MPUbase+1, bit 7, RXS is updated to reflect the new receive buffer FIFO state.

3. A write to the Command Register, MPUbase+1, of FFh will return the interface to non-UART mode.

4. All other writes to the Command Register, MPUbase+1, are ignored.

EXTERNAL PERIPHERAL PORT

An external peripheral port is provided for interfacing devices external to the CS4232. These may include the OPL3 or CS9233 synthesizer, CDROM interface, and Plug and Play E^2PROM.

The External Peripheral Port consists of the following signals: 8-bit data bus, 2 or 3 address lines, read strobe, write strobe, and reset signal.

Synthesizer Interface

The CS4232 supports the current FM type synthesizer chips such as the Yamaha OPL3, as well as the Crystal Semiconductor CS9233 wave table synthesizer chip. This interface consists of:

$\overline{\text{SCS}}$ - chip select
$\overline{\text{SINT}}$ - Synthesizer Interrupt

The other signals such as address bits, data strobes, data, and reset are provided by the External Peripheral Port. The interface allows the host computer to access up to eight I/O mapped locations. The synthesizer interface is compatible with the Adlib and Sound Blaster standards. The typical Adlib I/O address is SYNbase = 338h.

Since the typical FM interface only requires four I/O address and does not use an interrupt, the XA2 address and the $\overline{\text{SINT}}$ pins are multifunction pins that default to XCTL0 and XCTL1. To use XCTL0/XA2 as an address pin, the hardware resource data must be changed. See the *Hardware Configuration Data* section for more information. To use XCTL1/$\overline{\text{SINT}}$ as an interrupt for the synthesizer, a pulldown resistor must be placed on the $\overline{\text{XIOW}}$ pin.

Standard Adlib Synthesizer I/O Map

Address	Name	Type
SYNbase+0	FM Status	Read Only
SYNbase+0	FM Address 0	Write Only
SYNbase+1	FM Data 0	Write Only
SYNbase+2	FM Address 1	Write Only
SYNbase+3	FM Data 1	Read Only

CDROM Interface

The CS4232 provides a typical CDROM controller interface that is compatible with the Sony, Mitsumi, and with some external logic, the Panasonic CDROM drives. This interface includes a programmable chip select and on-chip hardware to map DMA and interrupt signals to the ISA bus.

The four CDROM interface pins are multifunction pins that default to the upper address bits SA12 - SA15. To use the pins as a CDROM interface, a pulldown resistor must be placed on $\overline{\text{XIOR}}$ ($\overline{\text{XIOR}}$ must be buffered if driving TTL logic). Secondly, the default address space for the peripheral port is 4 I/O locations with XCTL0/XA2 defaulting to the control pin XCTL0. To use XCTL0/XA2 as the XA2 address pin, thereby increasing the address range of the peripheral port to 8 locations, the hardware resource data must be changed. See the *Hardware Configuration Data* section.

SERIAL AUDIO DATA PORT

The WSS Codec includes a serial audio interface for transferring digital audio data between the CS4232 and a external serial device such as a DSP processor. The serial port connections exist on the #2 joystick inputs of the Game Port interface. Once the serial port operation is enabled, the second joystick function is no longer available.

The audio serial port is software enabled via the SPE bit in the WSS Codec indirect register I16. Once enabled, the data from the ADCs is sent to the SDOUT pin and the audio data input on the SDIN pin is routed to the DACs. The ISA interface is active in this mode to allow control of volume and format control. While the serial port is enabled, audio data may still be read from the ADCs over the ISA bus, but the DACs only accept data from the SDIN pin.

FSYNC and SCLK are always output from the CS4232 when the serial port is enabled. The serial port can be configured in one of three serial port formats, shown in Figures 6-8. SF1 and SF0 in I16 select the particular format. Both left and right audio words are always 16 bits wide with the audio data left justified. (i.e. ADPCM occupies the first four bits). Unused bits are output as zeros after the LSB. The justification is illustrated in Figure 5. When the mono audio format is selected, the right channel output is set to zero and the left channel input is sent to both DAC channels.

The first format - SPF0, shown in Figure 6, is called 64-bit enhanced. This format has 64 SCLK's per frame with a one bit period wide FSYNC that precedes the frame. The first 16 bits occupy the left word and the second 16 bits occupy the right word. The last 32 bits contain four status bits and 28 zeros. This is the only mode that contains status information.

The second serial format - SPF1, shown in Figure 7, is called 64-bit mode. This format also has 64 SCLK's per frame, but has FSYNC transitioning high at the start of the left data word and low at the start of the right data word. Both the left and right data words are followed by 16 zeros.

The third serial format - SPF2, shown in Figure 8, is called 32-bit mode. This format has 32 SCLKs per frame and FSYNC is high for the left channel and low for the right channel. The absolute time is similar to the other two modes but SCLK is stopped after the right channel is finished. SCLK is held stopped until the start of the next frame (stopped for 32 bit period times). This mode is useful for DSPs that do not want the interrupt overhead of the 32 unused bit periods. As an example, if a DSP serial word length is 16 bits, then four interrupts will occur in SPF0 and SPF1 modes. In mode SPF2 the DSP will only be interrupted twice.

WSS CODEC SOFTWARE DESCRIPTION

The WSS Codec must be in Mode Change Enable Mode (MCE=1) before any changes to the Interface Configuration register (I9) or the Sample Frequency (lower four bits) in the Fs & Playback Data Format registers (I8) are allowed. The actual audio data formats, which are the upper four bits of I8 for playback and I28 for capture, can be changed by setting MCE (R0) or PMCE/CMCE (I16) high. The exceptions are CEN and PEN which can be changed "on-the-fly" via programmed I/O writes to these bits. All outstanding DMA transfers must be completed before new values of CEN or PEN are recognized.

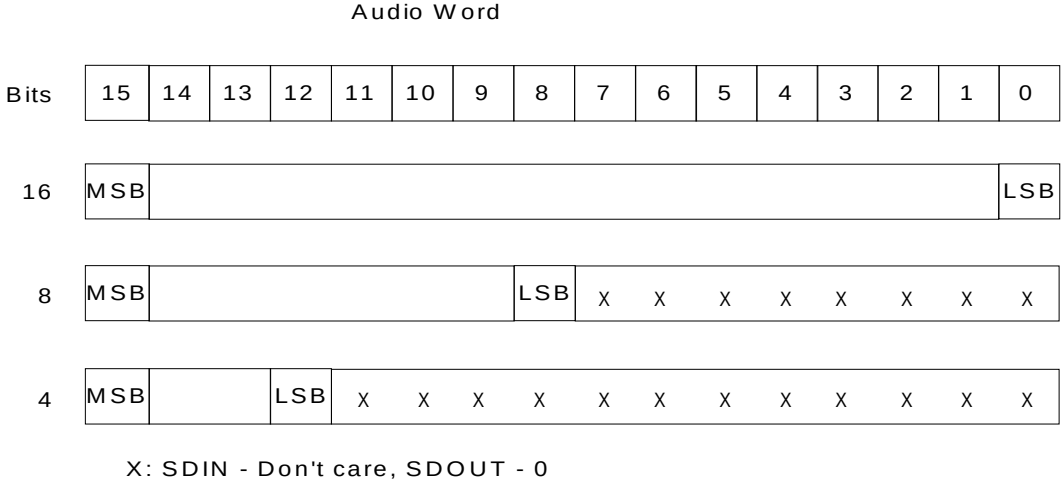


Figure 5. Serial Audio Data Justification

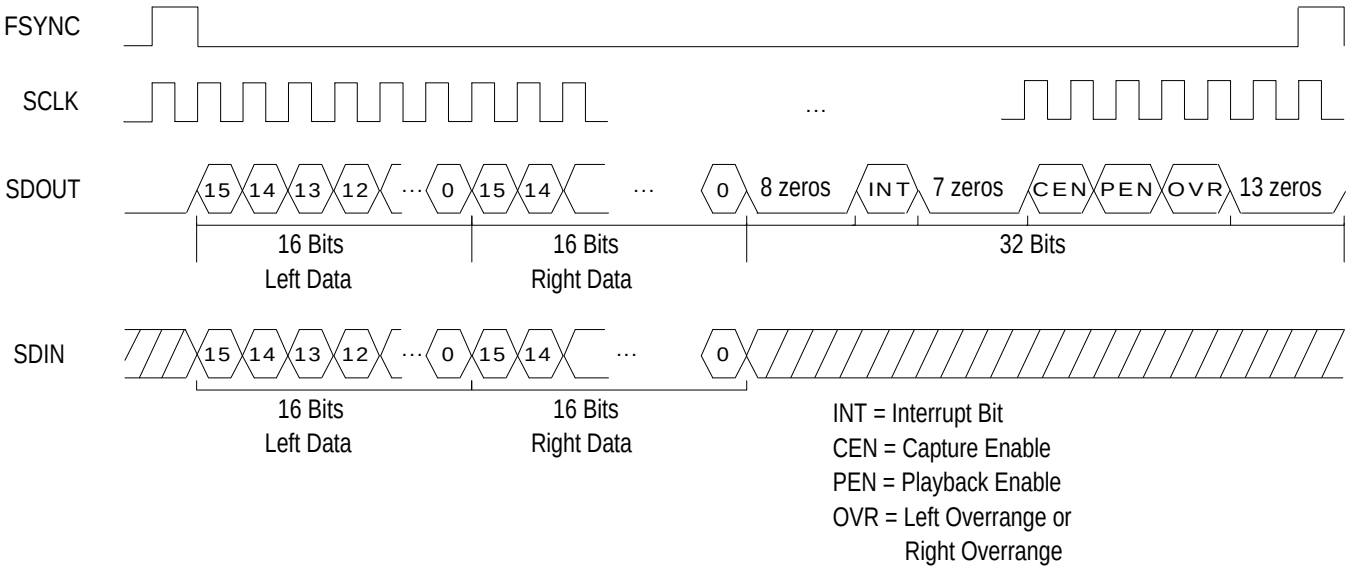


Figure 6. 64-bit Enhanced Mode (SF1,0 = 00)

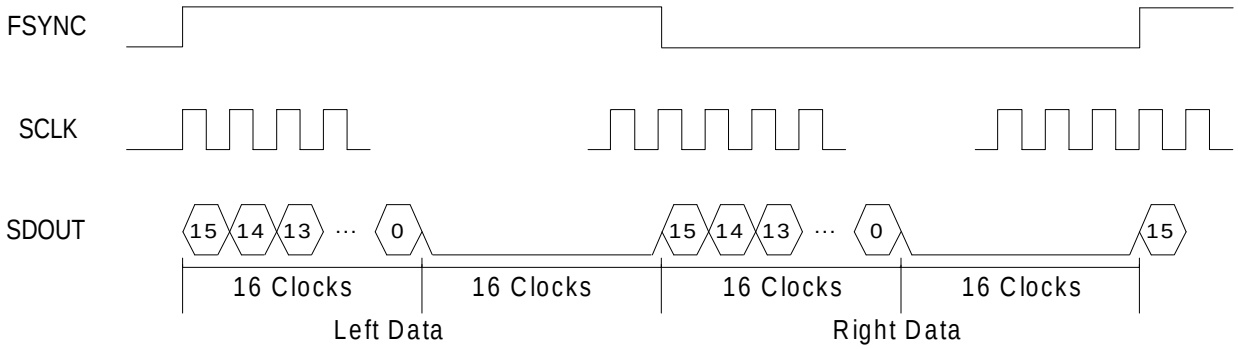


Figure 7. 64-bit Mode (SF1,0 = 01)

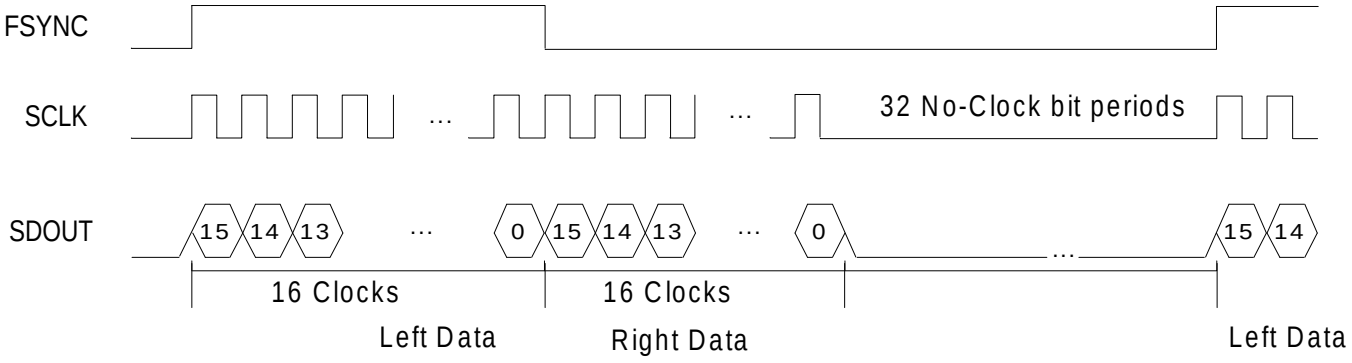


Figure 8. 32-bit Mode (SF1,0 = 10)

Calibration

The WSS Codec has four different calibration modes. The selected calibration occurs whenever the Mode Change Enable (MCE, R0) bit goes form 1 to 0

The completion of calibration can be determined by polling the Auto-Calibrate In-Progress bit in the Error Status and Initialization register (ACI, I11). This bit will be high while the calibration is in progress and low once completed. Transfers enabled during calibrate will not begin until the calibration cycle has completed.

The Calibration procedure is as follows:

1) Place the CS4232 in Mode Change Enable using the MCE bit of the Index Address register (R0).

2) Set the CAL1,0 bits in the Interface Configuration register (I9).

3) Return from Mode Change Enable by resetting the MCE bit of the Index Address register (R0).

4) Wait until 80h NOT returned

5) Wait until ACI (I11) cleared to proceed

NO CALIBRATION (CAL1,0 = 00)

This is the fastest mode since no calibration is performed. This mode is useful for games which require the sample frequency be changed quickly. This mode is also useful when the codec is operating full-duplex and an ADC data format change is desired. This is the only calibration mode that does not affect the DACs (i.e. mute the DACs). Changing from any other calibration mode to No Calibration mode will take 40 sample periods to complete; however, subsequent MCE cycles will take 0 sample periods. The FIFOs are not flushed in this calibration mode; therefore, MCE should not be enabled until the FIFOs are empty. If stale data is left in the FIFOs, and a data format change is made, the output could produce an audible pop.

CONVERTER CALIBRATION (CAL1,0 = 01)

This calibration mode calibrates the ADCs and the DACs, but does not calibrate any of the analog mixing channels. This is the second longest calibration mode, taking 136 sample periods. Because the analog mixer is not calibrated in this mode, any signals fed through the mixer will be unaffected. The calibration sequence is as follows:

The DACs are muted
The ADCs are calibrated
The DACs are calibrated
The DACs are unmuted

DAC CALIBRATION (CAL1,0 = 10)

This calibration mode only clears the DACs (playback) interpolation filters leaving the ADC unaffected. This is the second fastest calibration mode (no cal. is the fastest) taking 40 sample periods to complete. The calibration sequence is as follows:

The DACs are muted
The DAC filters are cleared
The DACs are unmuted

FULL CALIBRATION (CAL1, 0 = 11)

This calibration mode calibrates all offsets, ADCs, DACs, and analog mixers. Full calibration will be automatically be initiated on power up or anytime the CS4232 exits from a full power down state. This is the longest calibration mode and takes 168 sample periods to complete. The calibration sequence is as follows:

All outputs are muted (DACs and mixer)
The mixer is calibrated
The ADCs are calibrated
The DACs are calibrated
All outputs are unmuted

Changing Sampling Rate

The internal states of the WSS Codec are synchronized by the selected sampling frequency. The sample frequency can be set in one of two fashions. The standard WSS Codec method uses the Fs & Playback Data Format register (I8) to set the sample frequency. The changing of either the clock source or the clock frequency divide requires a special sequence for proper WSS Codec operation:

1) Place the WSS Codec in Mode Change Enable using the MCE bit of the Index Address register (R0).

2) During a single write cycle, change the Clock Frequency Divide Select (CFS) and/or Clock 2 Source Select (C2SL) bits of the Fs & Playback Data Format register (I8) to the desired value. (The data format may also be changed.)

3) The CS4232 resynchronizes its internal states to the new clock. During this time the CS4232 will be unable to respond at its parallel interface. Writes to the CS4232 will not be recognized and reads will always return the value 80 hex.

4) The host now polls the WSS Codec's Index Address register (R0) until the value 80 hex is no longer returned. Since both crystals are always running in the CS4232, 80h may occur to fast for ISA bus reads; therefore, it may never be seen by software.

5) Once the CS4232 is no longer responding to reads with a value of 80 hex, normal operation can resume and the CS4232 can be removed from MCE.

The C2SL and CFS bits cannot be changed unless the MCE bit has been set. Attempts to change the Data Format registers (I8, I28) or Interface Configuration register (I9, except CEN and PEN) without MCE set, will not be recognized.

A second method of changing the sample frequency is to disable the sample frequency bits in I8 (lower four bits) by setting SRE in I22. When this bit is set, OSM1 and OSM0 in I10, along with the rest of the bits in I22, are used to set the sample frequency. Once enabled, these bits can be changed without doing an MCE cycle. They also support a finer resolution of sample frequencies, albeit with a more complicated algorithm.

Changing Audio Data Formats

In MODE 1, MCE must be used to select the audio data format in I8. Since MCE causes a calibration cycle, it is not ideal for full-duplex operation. In MODE2, individual Mode Change Enable bits for capture and playback are provided in register I16. MCE (R0) must still be used to select the sample frequency, but PMCE (playback) and CMCE (capture) allow changing the respective data formats without causing a calibration to occur. Setting PMCE (I16) clears the playback FIFO and allows the upper four bits of I8 to be changed. Setting CMCE (I16) clears the capture FIFO and allows the upper four bits of I28 to be changed.

Audio Data Formats

In MODE 1 operation, all data formats of the WSS Codec are in "little endian" format. This format defines the byte ordering of a multibyte word as having the least significant byte occupying the lowest memory address. Likewise, the most significant byte of a little endian word occupies the highest memory address.

The sample frequency is always selected in the Fs & Playback Data Format register (I8). In

MODE 1 the same register, I8, determines the audio data format for both playback and capture; however, in MODE 2, I8 only selects the playback data format and the capture data format is independently selectable in the Capture Data Format register (I28).

The WSS Codec always orders the left channel data before the right channel. Note that these definitions apply regardless of the specific format of the data. For example, 8-bit linear data streams look exactly like 8-bit companded data streams. Also, the left sample always comes first in the data stream regardless of whether the sample is 16-bit or 8-bit in size.

There are four data formats supported by the WSS Codec during MODE 1 operation: 16-bit signed (little endian), 8-bit unsigned, 8-bit companded μ-Law, and 8-bit companded A-Law. See Figures 11-14.

Additional data formats are supported in MODE 2 operation: 4-bit ADPCM, and 16-bit signed Big Endian. See Figures 15 through 18. With the addition of the Big Endian and ADPCM audio data formats, the CS4232 is compliant with the IMA recommendations for digital audio data formats (and sample frequencies).

16-BIT SIGNED

The 16-bit signed format (also called 16-bit 2's complement) is the standard method of representing 16-bit digital audio. This format gives 96 dB theoretical dynamic range and is the standard for compact disk audio players. This format uses the value -32768 (8000h) to represent maximum negative analog amplitude, 0 for center scale, and 32767 (7FFFh) to represent maximum positive analog amplitude.

8-BIT UNSIGNED

The 8-bit unsigned format is commonly used in the personal computer industry. This format delivers a theoretical dynamic range of 48 dB. This format uses the value 0 (00h) to represent maximum negative analog amplitude, 128 for center scale, and 255 (FFh) to represent maximum positive analog amplitude. The 16-bit signed and 8-bit unsigned transfer functions are shown in Figure 9.

8-BIT COMPANDED

The 8-bit companded formats (A-Law and μ-Law) come from the telephone industry. μ-Law is the standard for the United States/Japan while A-Law is used in Europe. Companded audio al-

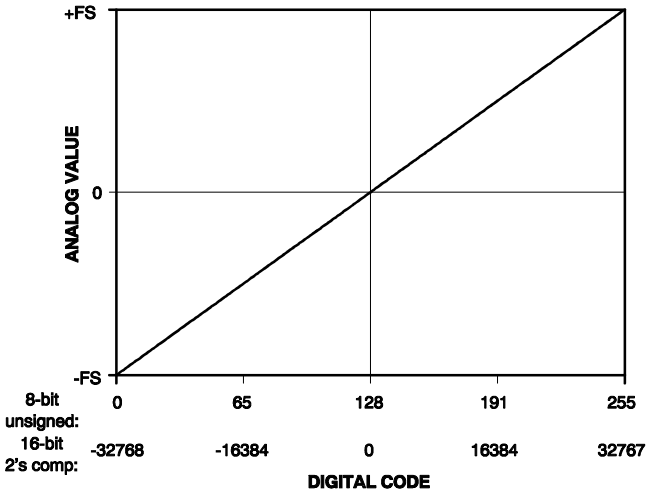


Figure 9. Linear Transfer Functions

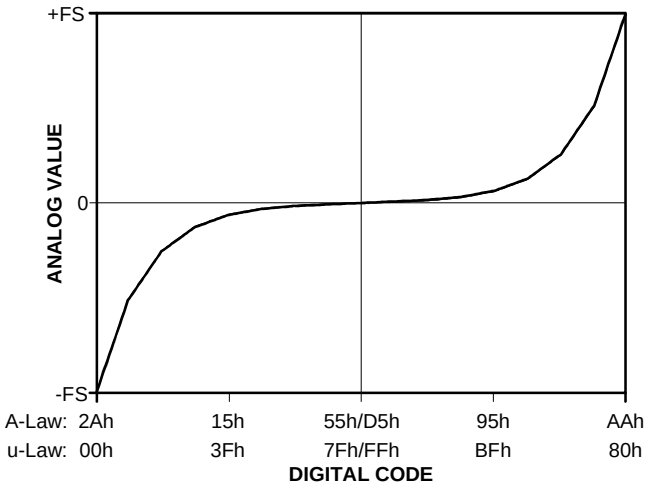


Figure 10. Companded Transfer Functions

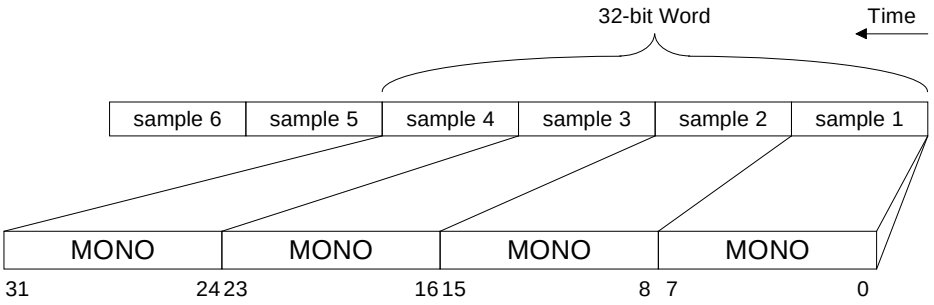


Figure 11. 8-bit Mono, Unsigned Audio Data

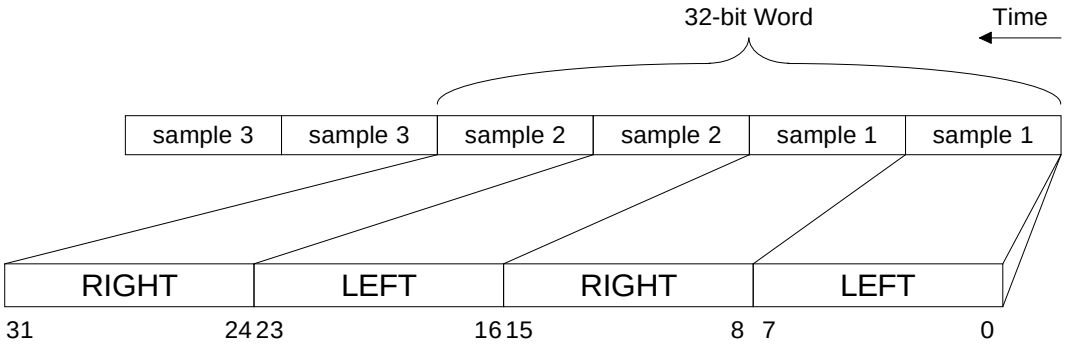


Figure 12. 8-bit Stereo, Unsigned Audio Data

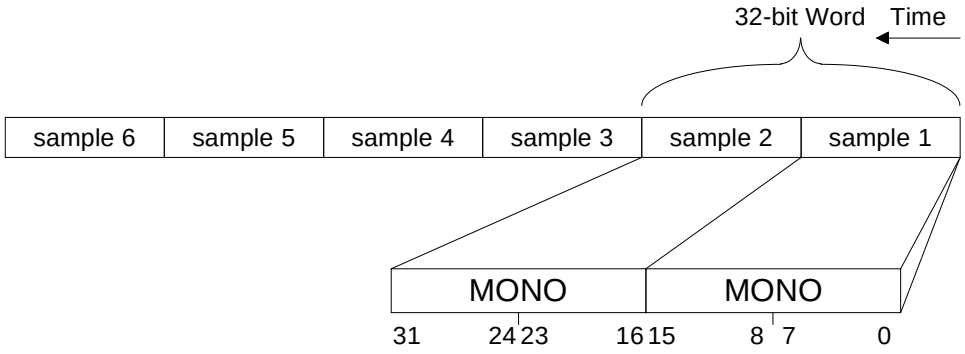


Figure 13. 16-bit Mono, Signed Little Endian Audio Data

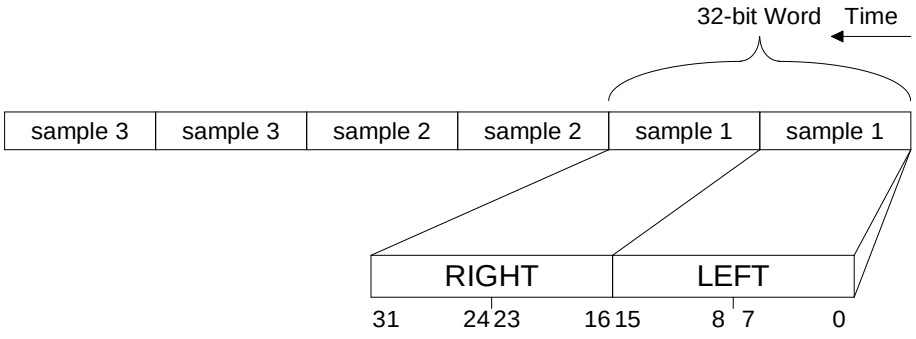


Figure 14. 16-bit Stereo, Signed Little Endian Audio Data

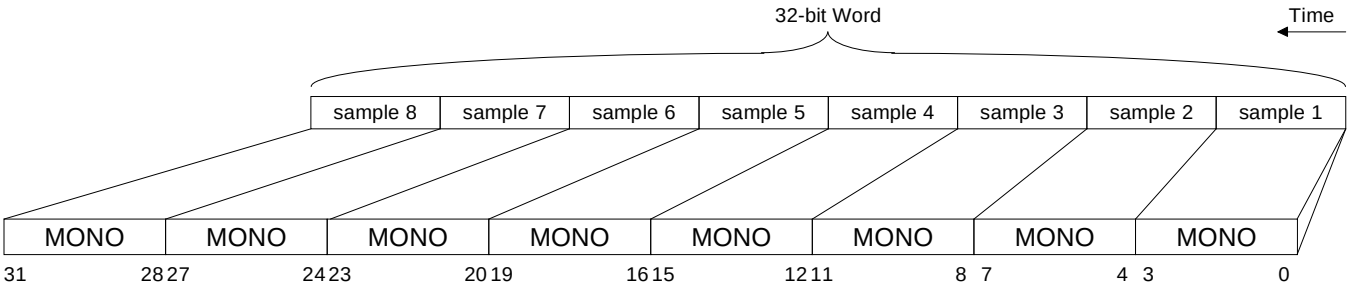


Figure 15. 4-bit Mono, ADPCM Audio Data

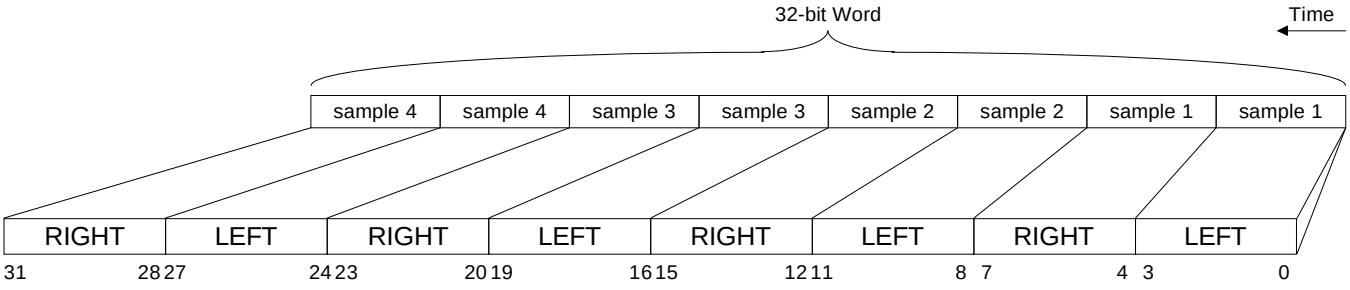


Figure 16. 4-bit Stereo, ADPCM Audio Data

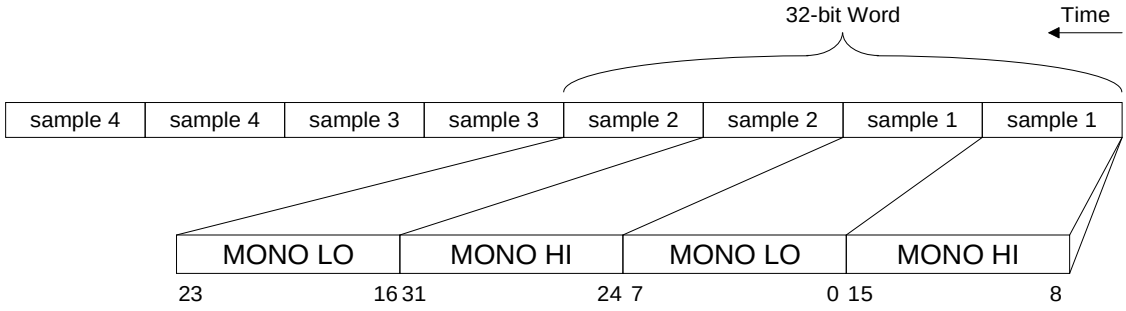


Figure 17. 16-bit Mono, Signed Big Endian Audio Data

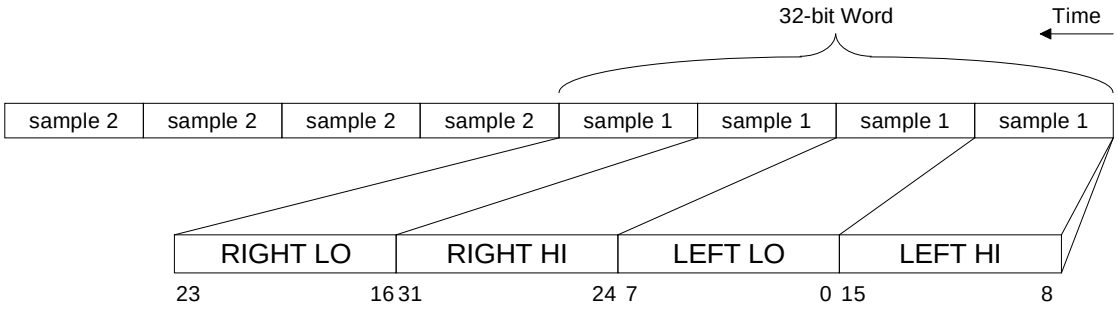


Figure 18. 16-bit Stereo, Signed Big Endian Audio Data

lows either 64 dB or 72 dB of dynamic range using only 8-bits per sample. This is accomplished using a non-linear companding transfer function which assigns more digital codes to lower amplitude analog signals with the sacrifice of precision on higher amplitude signals. The μ-Law and A-Law formats of the WSS Codec conform to the CCITT G.711 specifications. Figure 10 illustrates the transfer function for both A- and μ-Law. Please refer to the standards mentioned above for an exact definition.

ADPCM COMPRESSION/DECOMPRESSION

In MODE 2, the WSS Codec also contains Adaptive Differential Pulse Code Modulation (ADPCM) for improved performance and compression ratios over μ-Law or A-Law. The ADPCM format is compliant with the IMA standard and provides a 4-to-1 compression ratio (i.e. 4 bits are saved for each 16-bit sample captured). For more information on the specifics of the format, contact the IMA at (410) 626-1380. Figures 15 and 16 illustrate the ADPCM data flow.

The ADPCM format is unique with respect to the FIFO depth and the DMA Base register value. The ADPCM format fills the FIFOs completely (64 bytes); therefore, the FIFOs hold 64 stereo samples and 128 mono samples. When samples are being transferred using DMA, the DMA request stays active for four bytes, similar to the 16-bit stereo data mode. In PIO mode, the Status register (R2) indicates which of the four bytes is being transferred.

When CEN is 0 (capture disabled), the ADPCM block's accumulator and step size are cleared. When CEN is enabled, the ADPCM block will start converting. Care should be taken to insure that the "overrun" condition never occurs, otherwise the data may not be constructed properly upon playback. If pausing the capture sequence is desired, the ADPCM Capture Freeze bit (ACF, I23) should be set. When this bit is set, the ADPCM algorithm will continue to operate until a complete word (4 bytes) is written to the FIFO. Then the ADPCM's block accumulator and step size will be frozen. The software must continue reading until the FIFO is empty, at which time the requests will stop. When ACF is cleared, the ADPCM adaptation will continue.

When PEN is 0 (playback disabled), the ADPCM block's accumulator and step size are cleared. When PEN is set, the ADPCM block will start converting. When pausing the playback stream is desired, audio data should not be sent to the codec, causing an underrun. This can be accomplished by disabling the DMA controller or not sending data in PIO mode. The underrun will be detected by the WSS Codec and the adaptation will freeze. When data is sent to the codec, adaptation will resume. It is critical that all playback ADPCM samples are sent to the codec, since dropped samples will cause errors in adaptation. Whereas toggling PEN resets the accumulator and step size, the APAR bit (I17) only resets the accumulator without affecting the step size.

DMA Registers

The DMA registers allow easy integration of the CS4232 into ISA systems. Peculiarities of the ISA DMA controller require an external count mechanism to notify the host CPU of a full DMA buffer via interrupt. The programmable DMA Base registers provide this service.

The act of writing a value to the Upper Base register causes both Base registers to load the Current Count register. DMA transfers are enabled by setting the PEN/CEN bit while PPIO/CPIO is clear. (PPIO/CPIO can only be changed while the MCE bit is set.) Once transfers are enabled, each sample that is transferred by a DMA cycle will decrement the Current Count register (with the exception of the ADPCM format) until zero is reached. The next

sample after zero generates an interrupt and reloads the Current Count registers with the values in the Base registers.

For all data formats except ADPCM, the DMA Base registers must be loaded with the number of samples, minus one, to be transferred between "DMA Interrupts". Stereo data contains twice as many samples as mono data; however, 8-bit data and 16-bit data contain the same number of samples. Symbolically:

$$\text{DMA Base register}_{16} = N_S - 1$$

Where N_S is the number of samples transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

For the ADPCM data format, the contents of the DMA Base registers is calculated differently from any other data format. The Base registers must be loaded with the number of BYTES to be transferred between "DMA interrupts", divided by four, minus one. The same equation is used whether the data format is stereo or mono ADPCM. Symbolically:

$$\text{DMA Base register}_{16} = N_b/4 - 1$$

Where N_b is the number of BYTES transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

PLAYBACK DMA REGISTERS

The playback DMA registers (I14/15) are used for sending playback data to the DACs in MODE 2. In MODE 1, these registers (I14/15) are used for both playback and capture; therefore, full-duplex DMA operation is not possible.

When the playback Current Count register rolls under, the Playback Interrupt bit, PI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Playback Interrupt bit, PI (I24).

CAPTURE DMA REGISTERS

The Capture DMA Base registers (I30/31) provide a second pair of Base registers that allow full-duplex DMA operation. With full-duplex operation capture and playback can occur simultaneously. These registers are provided in MODE 2 operation only.

When the capture Current Count register rolls under, the Capture Interrupt bit, CI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Capture Interrupt bit, CI (I24).

Digital Loopback

Digital Loopback is enabled via the LBE bit in the Loopback Control register (I13). This loopback routes the digital data from the ADCs to the DACs. This loopback can be digitally attenuated via additional bits in the Loopback Control register (I13). Loopback is then summed with DAC data supplied at the digital bus interface. When loopback is enabled, it will "freerun" synchronous with the sample rate. The digital loopback is shown in the CS4232 Block Diagram at the beginning of this data sheet. This loopback can be used to mix the incoming microphone data with data from the DACs. Since the WSS Codec allows selection of different data formats between capture and playback, if the capture channel is set to mono and the playback channel set to stereo, the mono input (mic) data will be mixed into both channels of the output mixer.

If the sum of the loopback and bus data are greater than full scale, WSS Codec will send the appropriate full scale value to the DACs (clipping).

Timer Registers

The Timer registers are provided for synchronization, watch dog and other functions where a high resolution time reference is required. This counter is 16 bits and the exact time base, listed in the register description, is determined by the crystal selected.

The Timer register is set by loading the high and low registers to the appropriate values and setting the Timer Enable bit, TE, in the Alternate Feature Enable register (I16). This value will be loaded into an internal Current Count register and will decrement at approximately a 10 µsec rate. When the value of the Current Count register reaches zero, an interrupt will be posted to the host and the Timer Interrupt bit, TI, is set in the Alternate Feature Status register (I24). On the next timer clock the value of the Timer registers will be loaded into the internal Current Count register and the process will begin again. The interrupt is cleared by any write to the Status register (R2) or by writing a "0" to the Timer Interrupt bit, TI, in the Alternate Feature Status register (I24).

WSS Codec Interrupt

The INT bit of the Status register (R2) always reflects the status of the WSS Codec's internal interrupt state. A roll-over from any Current Count register (DMA playback, DMA capture, or Timer) sets the INT bit. This bit remains set until cleared by a write of ANY value to Status register (R2), or by clearing the appropriate bit or bits (PI, CI, TI) in the Alternate Feature Status register (I24).

The Interrupt Enable (IEN) bit in the Pin Control register (I10) determines whether the interrupt assigned to the WSS Codec responds to the interrupt event. When the IEN bit is low, the interrupt is masked and the IRQ pin assigned to the WSS Codec is held low. However, the INT bit in the Status register (R2) always responds to the counter.

Error Conditions

Data overrun or underrun could occur if data is not supplied to or read from the WSS Codec in an appropriate amount of time. The amount of time for such data transfers depends on the frequency selected within the WSS Codec.

Should an overrun condition occur during data capture, the last whole sample (before the overrun condition) will be read by the DMA interface. A sample will not be overwritten while the DMA interface is in the process of transferring the sample.

Should an underrun condition occur in a playback case the last valid sample will be output (assuming DACZ = 0) to the digital mixer. This will mask short duration error conditions. When the next complete sample arrives from the host computer the data stream will resume on the next sample clock.

DIGITAL HARDWARE DESCRIPTION

The best example of hardware connection for the different sections of the CS4232 such as joystick connector, ISA bus, and peripheral port connections is the CRD4232-1 reference design. This is a low-cost two-layer ISA card that supports all the features of the CS4232. The CRD4232-1 Data Sheet contains all the schematics, layout plots and a Bill of Materials; thereby providing a complete example.

Bus Interface

The CS4232 ISA bus interface is capable of driving a 24mA data bus load and therefore does not require any external data bus buffering. See the CRD4232-1 Reference Design for a typical connection diagram.

FM Synthesis

If the external synthesizer is not a high quality wave-table synthesizer such as the CS9233, then an FM synthesizer is needed to support the synthesis portion of the Windows Sound System and Sound Blaster Compatible interfaces. The synthesizer has a chip select, $\overline{SCS}$, and an optional interrupt $\overline{SINT}$ which is multiplexed with the control pin XCTL1. Since the FM synthesizer interrupt is typically not used, the pin defaults to XCTL1. To change the pin to support $\overline{SINT}$, see the *Multiplexed Pin Configuration* section. The rest of the synthesizer interface uses the external peripheral port pins which include address and data lines, along with a read strobe, write strobe, and an active low reset pin. Figure 19 illustrates an example circuit that uses the OPL3L from Yamaha for FM synthesis, with the Crystal CS4333 8-pin DAC. Since the OPL3L requires a 33 MHz fundamental-mode crystal - which is not easily obtainable - the Micro Clock MK1420S is used for clock generation. This chip takes the 14 MHz signal from a crystal or the ISA bus, and generates the clocks needed by the OPL3L as well as the CS4232.

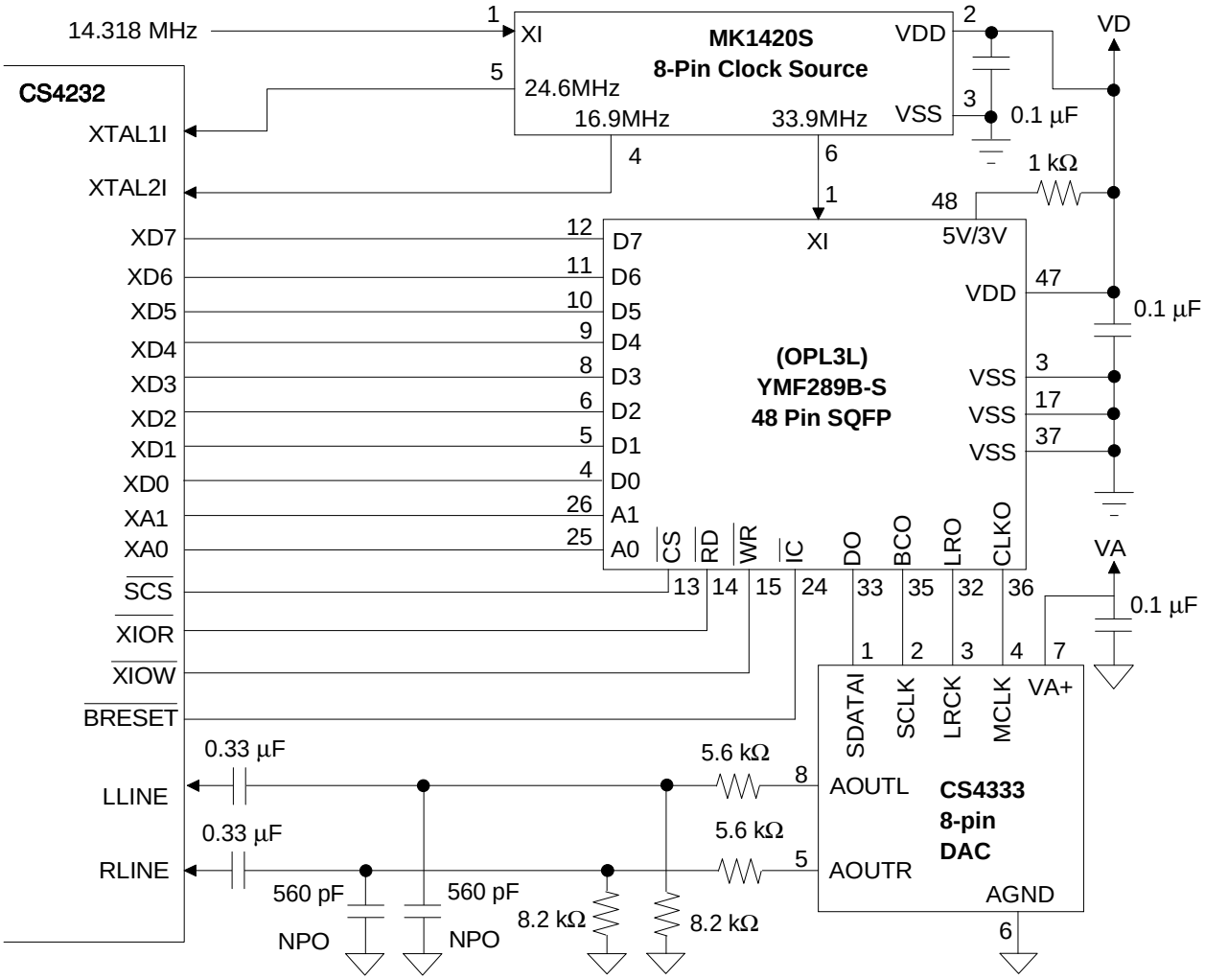


Figure 19. FM Synthesis Circuit

Crystals / Clocks

Four pins have been allocated to allow the interfacing of two crystal oscillators to the CS4232: XTAL1I, XTAL1O, XTAL2I, XTAL2O. The crystals should be designed as fundamental mode, parallel resonant, with a load capacitor of between 10 and 20 pF. The capacitors connected to each of the crystal pins should be twice the load capacitance specified to the crystal manufacturer. The XTAL1 oscillator is designed with slightly more gain to handle higher frequencies, but any crystal with the above specifications should suffice. The standard crystals for audio are:

XTAL1: 24.576 MHz
Fundamental Mode
Parallel Resonant, C_L = 20 pF

XTAL2: 16.9344 MHz
Fundamental Mode
Parallel Resonant, C_L = 20 pF

These crystal frequencies support the standard sample frequencies listed in Table 10.

External CMOS clocks may be connected to the crystal inputs (XTAL1I, XTAL2I) in lieu of the crystals. When using external CMOS clocks, the XTAL out pins should be left floating. Extreme care should be used when laying out a board using external clocks since coupling between clocks can degrade analog performance.

General Purpose Output Pins

Two general purpose outputs are provided to enable control of circuitry external to the CS4232 (i.e. mute function). XCTL1 and XCTL0 in the WSS Codec register I10 are output directly to the appropriate pin when enabled.

Pin XCTL0/XA2 becomes an output for XCTL0 whenever the resource data for the CDROM or Synthesizer specifies a logical device address range that is four bytes. If the address range is specified to be eight bytes, then XA2 becomes an output for SA2 from the ISA bus.

Pin XCTL1/$\overline{\text{SINT}}$ becomes an output for XCTL1 when the state of the $\overline{\text{XIOW}}$ pin is sampled high during a high to low transition of the RESDRV pin. If $\overline{\text{XIOW}}$ is sampled low, $\overline{\text{SINT}}$ becomes an input for the Synthesizer interrupt. $\overline{\text{XIOW}}$ has an internal pullup resistor.

Reset and Power Down

A RESDRV pin places the CS4232 into maximum power conservation mode. When RESDRV goes high, the PnP registers are reset - all logical devices are disabled, all analog outputs are muted, and the voltage reference then slowly decays to ground. When RESDRV is brought low, an initialization procedure begins which causes a full calibration cycle to occur. While the WSS Codec is initializing, any reads from the WSS interface will return 80 hex and writes will be ignored. When initialization is completed, the registers will contain their reset value as stated in the register section of the data sheet and the part will be isolated from the bus.

Software low-power states are available through bits in the Control logical device register space. These power-down modes retain all the internal registers such that the chip will be ready for operation, immediately after power up, without having to re-program the registers.

Multiplexed Pin Configuration

On the high to low transition of the RESDRV pin, the CS4232 samples the state of the $\overline{\text{XIOR}}$ and $\overline{\text{XIOW}}$ pins. Both of these pins have internal 100kΩ pullups to +5V. If either of these pins is pulled low externally, they must be buffered before connecting to a TTL input (as in a CDROM port) since TTL cannot be pulled low.

The state of $\overline{\text{XIOR}}$ at the time RESDRV is brought low determines the function of the

CDROM interface pins. If $\overline{\text{XIOR}}$ is sampled low (external pulldown) then $\overline{\text{CDCS}}$, $\overline{\text{CDACK}}$, CDINT, CDRQ become the standard CDROM interface pins. If $\overline{\text{XIOR}}$ is sampled high, then $\overline{\text{CDCS}}$, $\overline{\text{CDACK}}$, CDINT, CDRQ are used to input SA12, SA13, SA14, SA15 respectively.

The state of $\overline{\text{XIOW}}$ at the time RESDRV is brought low determines the function of the XCTL1/$\overline{\text{SINT}}$ pin. If $\overline{\text{XIOW}}$ is sampled low (external pulldown) then XCTL1/$\overline{\text{SINT}}$ functions as an input for the synthesizer interrupt. If $\overline{\text{XIOW}}$ is sampled high (pin left unconnected) then XCTL1/$\overline{\text{SINT}}$ becomes an output for XCTL1.

ANALOG HARDWARE DESCRIPTION

The analog hardware consist of an MPC Level 2-compatible mixer (four stereo mix sources), three line-level stereo inputs, a stereo microphone input, a mono input, a mono output, and a stereo line output. This section describes the analog hardware needed to interface with these pins.

Line-Level Inputs Plus MPC Mixer

The analog inputs consist of four stereo analog inputs, and one mono input. As shown on this data sheet cover, the input to the ADCs comes from a multiplexer that selects between two analog line-level inputs (LINE, AUX1), a microphone level input (MIC), and the output from the MPC-compatible mixer. The LINE and AUX1 lines also feed the MPC mixer and include individual volume controls. Unused analog inputs should be connected together and then connected through a capacitor to analog ground.

The analog input interface is designed to accommodate four stereo inputs and one mono input. Three of these sources are multiplexed to the ADC. These inputs are: a stereo line-level input (LINE), a stereo microphone input (MIC), and a stereo auxiliary line-level input (AUX1). The LINE and AUX1 inputs have a separate path, with volume control, to the output analog mixer which has the additional inputs of a stereo AUX2 channel, a mono input channel, and the output of the DACs. All audio inputs should be capacitively coupled to the CS4232.

To obtain Sound Blaster mixer compatibility, the mapping of external devices to analog inputs is important. The external FM or Wave-Table synthesizer analog outputs must be connected to the LINE inputs. The CDROM analog outputs must be connected to the AUX2 inputs, and the external Line Inputs must be connected to the AUX1 analog inputs.

Since some analog inputs can be as large as 2 V_{RMS}, the circuit shown in Figure 20 can be used to attenuate the analog input to 1 V_{RMS} which is the maximum voltage allowed for the line-level inputs on the CS4232.

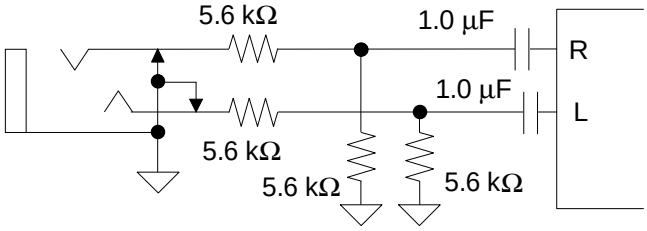


Figure 20. Line Inputs

Microphone Level Inputs

The microphone level inputs, LMIC and RMIC, include a selectable +20dB gain stage for interfacing to an external microphone. The 20dB gain block can be turned off to provide another stereo line-level input. Figure 21 illustrates a single-ended microphone input buffer circuit that will support lower gain mics. If a mono microphone is all that is desired, the RMIC input should be connected to the output of the mono op amp, used for LMIC, through its own AC coupling capacitor.

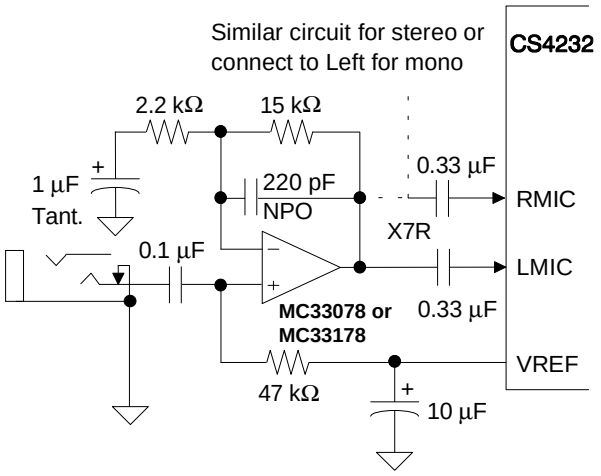


Figure 21. Left or Mono Microphone Input

Mono Input

The mono input, MIN, is useful for mixing the output of the "beeper" (timer chip), provided in all PCs, with the rest of the audio signals. The attenuation control allows 16 levels in -3dB steps. In addition, a mute control is provided. The attenuator is a single channel block with the resulting signal sent to the output mixer where it is mixed with the left and right outputs. Figure 22 illustrates a typical input circuit for the Mono In. If MIN is driven from a CMOS gate, the 4.7kΩ should be tied to AGND instead of VA+. Although this input is described for a low-quality beeper, the input is of the same high-quality as all other analog inputs and may be used for other purposes. At power-up, the MIN line is connected directly to the MOUT pin (with 9 dB of attenuation) allowing the initial beeps, heard when the computer is initializing, to pass through.

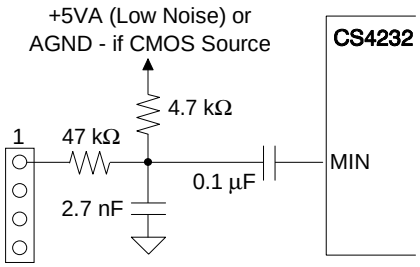


Figure 22. Mono Input

Line Level Outputs

The analog output section of the CS4232 provides a stereo line-level output. The other output types (headphone and speaker) can be implemented with external circuitry. LOUT and ROUT outputs should be capacitively coupled to external circuitry. Both LOUT and ROUT need 1000 pF NPO capacitors between the pin and AGND.

Mono Output with Mute Control

The mono output, MOUT, is a sum of the left and right output channels, attenuated by 6dB to prevent clipping at full scale. The mono out channel can be used to drive the PC-internal mono speaker using an appropriate drive circuit. This approach allows the traditional PC-sounds to be integrated with the rest of the audio system. Figure 23 illustrates a typical speaker driver circuit. The mute control is independent of the line outputs allowing the mono channel to mute the speaker without muting the line outputs. The power-up default has MIN connected to MOUT providing a pass-through for the beeps heard at power-up.

Miscellaneous Analog Signals

The LFILT and RFILT pins must have a 1000 pF NPO capacitor to analog ground. These capacitors, along with an internal resistor, provide a single-pole low-pass filter used at the inputs to the ADCs. By placing these filters at the input to the ADCs, low-pass filters at each analog input pin are avoided.

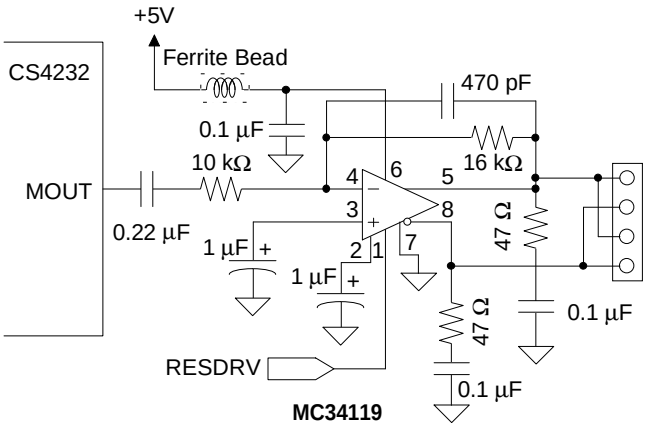


Figure 23. Mono Output

The REFFLT pin is used to lower the noise of the internal voltage reference. A 10µF and 0.1µF capacitor to analog ground should be connected with a short wide trace to this pin. No other connection should be made, as any coupling onto this pin will degrade the analog performance of the codec. Likewise, digital signals should be kept away from REFFLT for similar reasons.

The VREF pin is typically 2.1 V and provides a common mode signal for single-supply external circuits. VREF only supports light DC loads and should be buffered if AC loading is needed. For typical use, a 0.47 µF capacitor should be connected to VREF. High-gain microphone circuits can be improved by increasing the capacitance to 10 µF.

GROUNDING AND LAYOUT

Figure 24 is a suggested layout for the CS4232. Similar to other Crystal codecs, it is recommended that the device be located on a separate analog ground plane. With the CS4232's parallel data interface, however, optimum performance is achieved by extending the digital ground plane across pins 17 and 54. Pins 18, 46, and 53 are grounds for the data bus and should be electrically connected to the digital ground plane which will minimize the effects of the bus interface due to transient currents during bus switching. Figure 25 shows the recommended positioning of the decoupling capacitors. The capacitors must be on the same layer as, and close to, the CS4232. The vias shown go through to the ground plane layer. Vias, power supply traces, and VREF traces should be as large as possible to minimize the impedance.

POWER SUPPLIES

The power supply providing analog power should be as clean as possible to minimize coupling into the analog section and degrading analog performance. The VD1 and VD2 pins are isolated from the rest of the power pins and provide digital power for the asynchronous parallel bus. These two pins can be connected directly to the digital power supply. VDF1 through VDF3 provide power to internal sections of the codec and should be quieter than VD1 and VD2. This can be achieved by using a ferrite bead as shown in the CRD4232-1 Reference Design Data Sheet. Grounding is covered in the *Grounding and Layout* section.

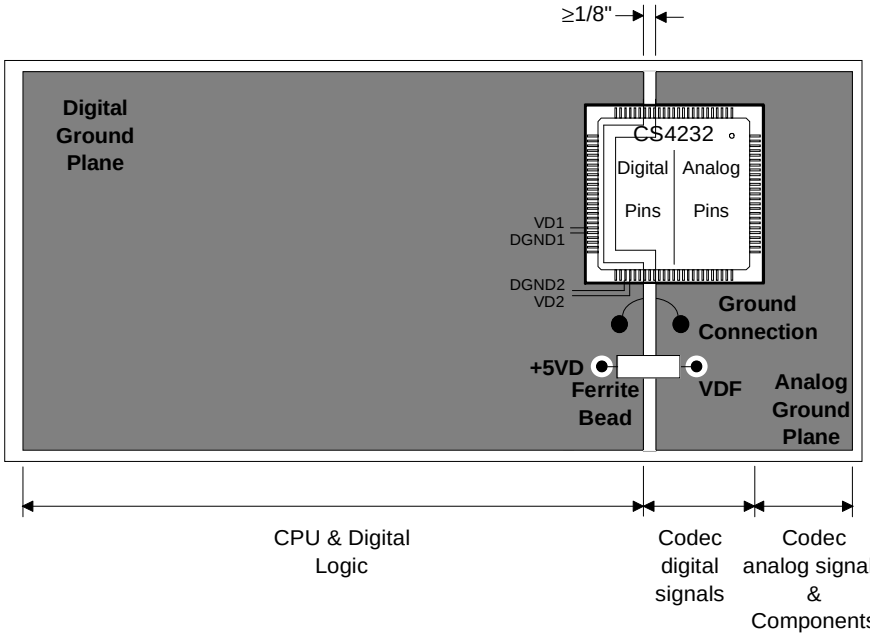


Figure 24. Suggested Layout Guideline

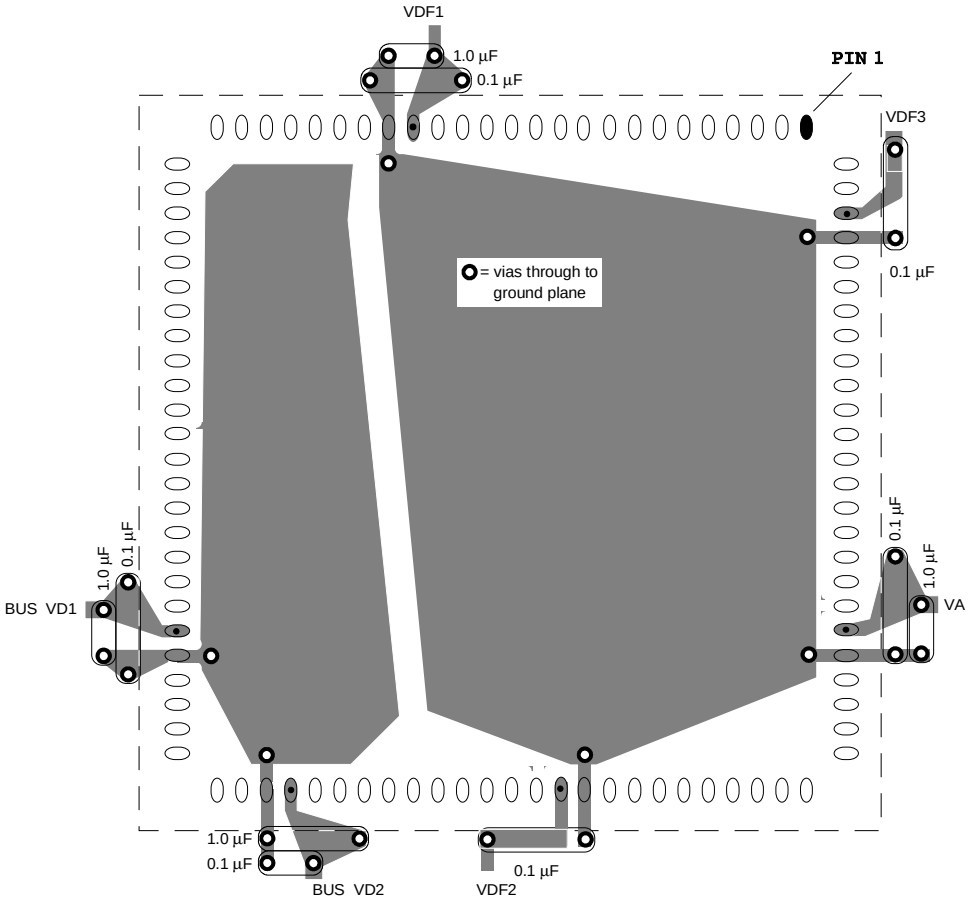


Figure 25. Recommended Decoupling Capacitor Positions

ADC/DAC FILTER RESPONSE PLOTS

Figures 26 through 31 show the overall frequency response, passband ripple, and transition band for the CS4232 ADCs and DACs. Figure 32 shows the DACs' deviation from linear phase. Since the CS4232 scales filter response based on sample frequency selected, all frequency response plots x-axis' are shown from 0 to 1 where 1 is equivalent to Fs. Therefore, for any given sample frequency, multiply the x-axis values by the sample frequency selected to get the actual frequency.

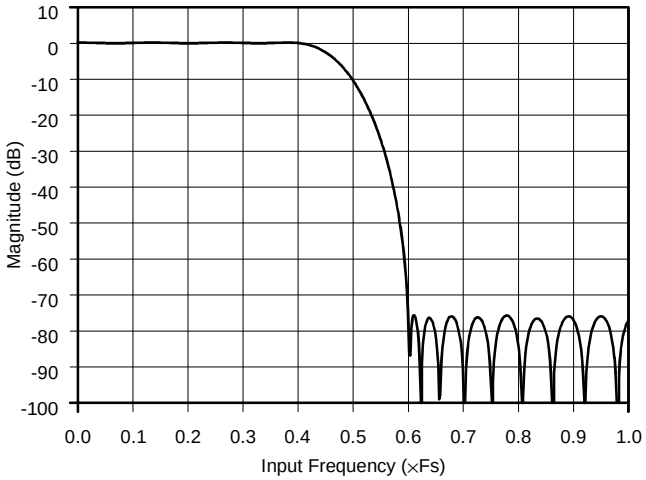


Figure 26. ADC Filter Response

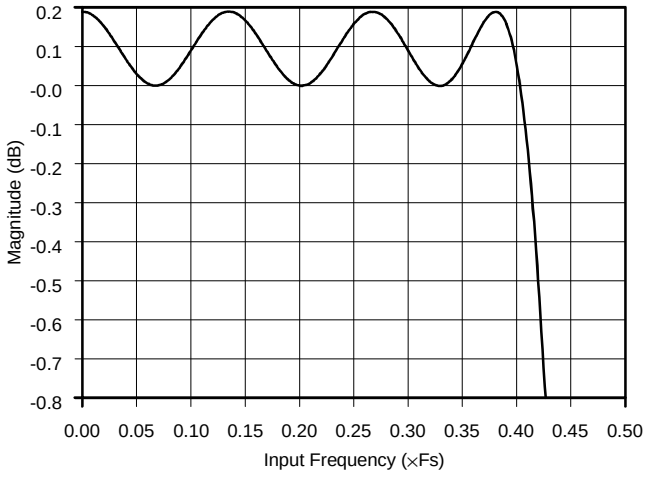


Figure 27. ADC Passband Ripple

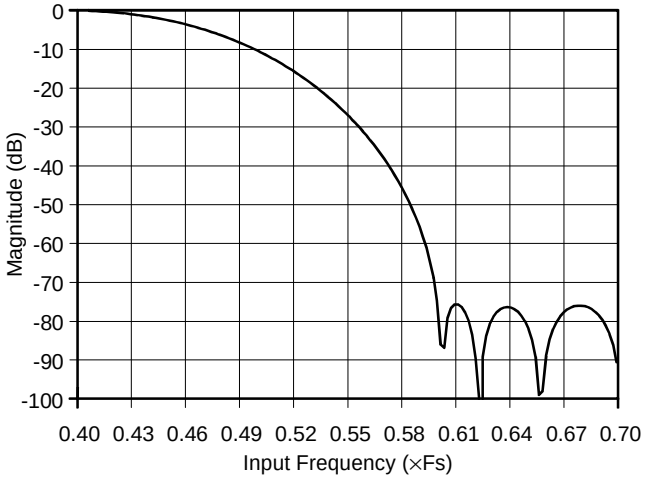


Figure 28. ADC Transition Band

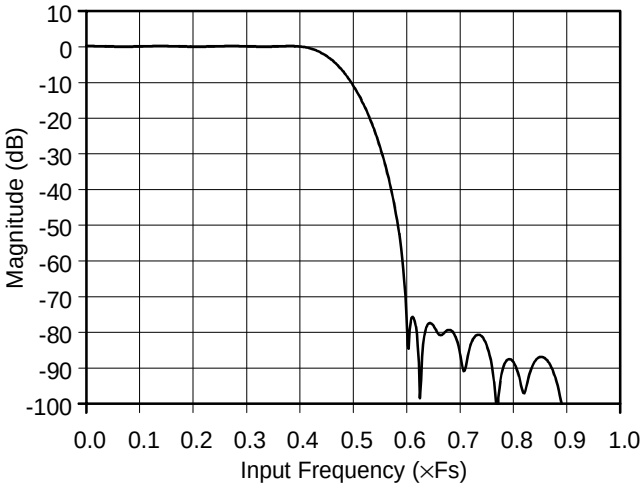


Figure 29. DAC Filter Response

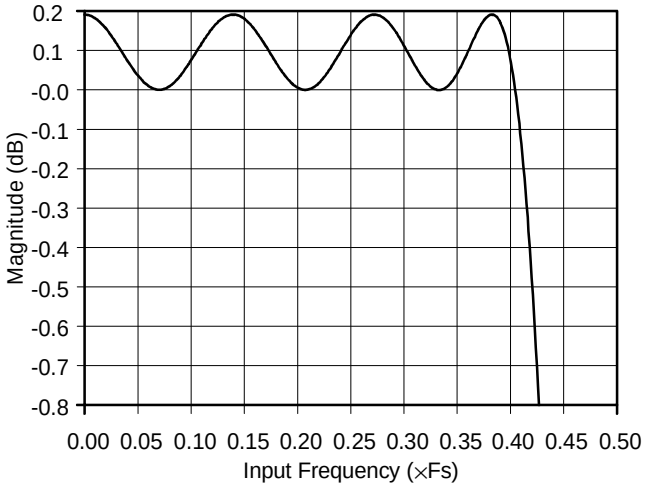


Figure 30. DAC Passband Ripple

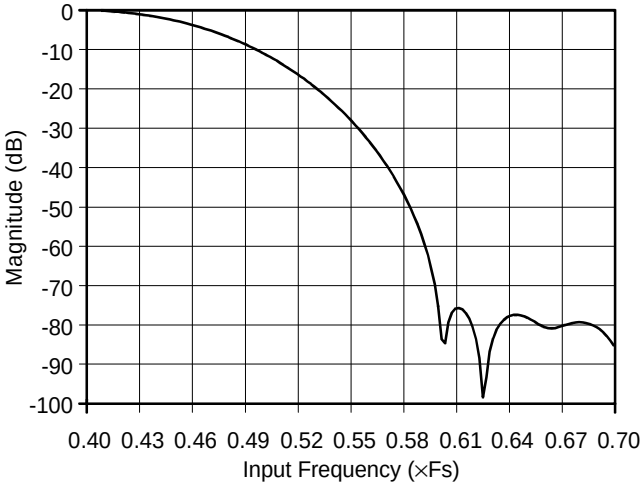


Figure 31. DAC Transition Band

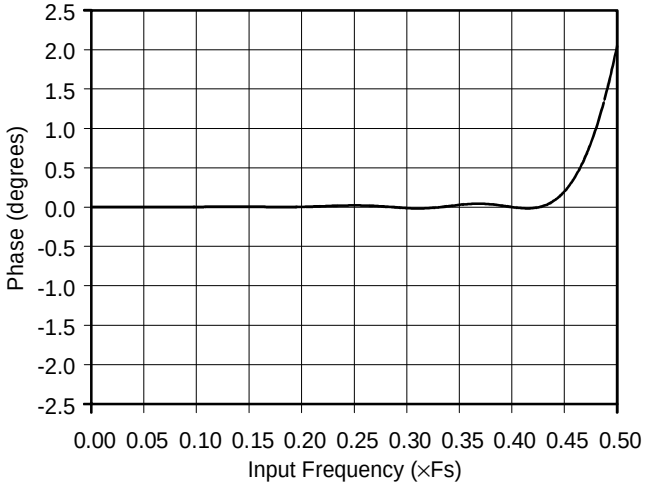
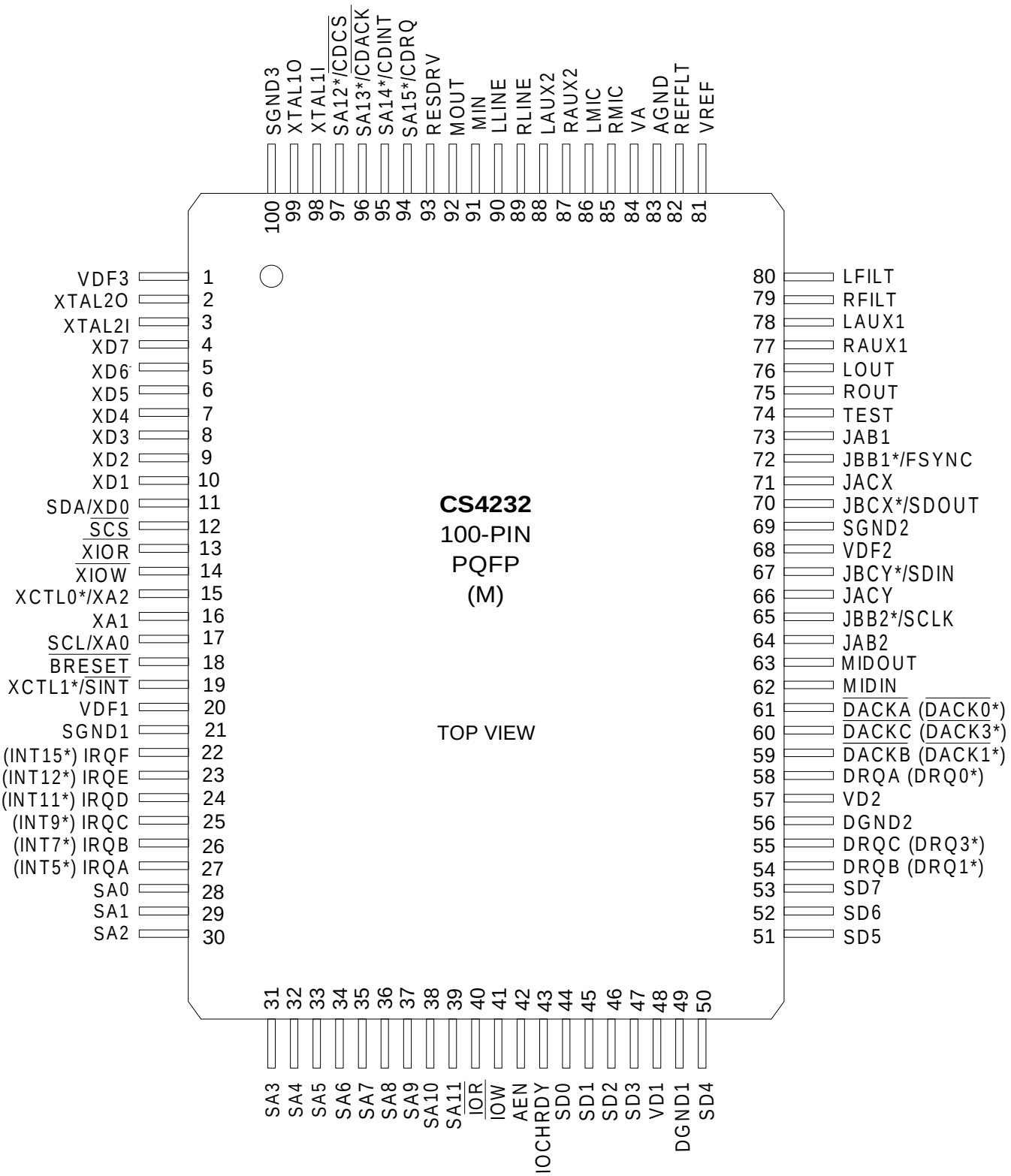
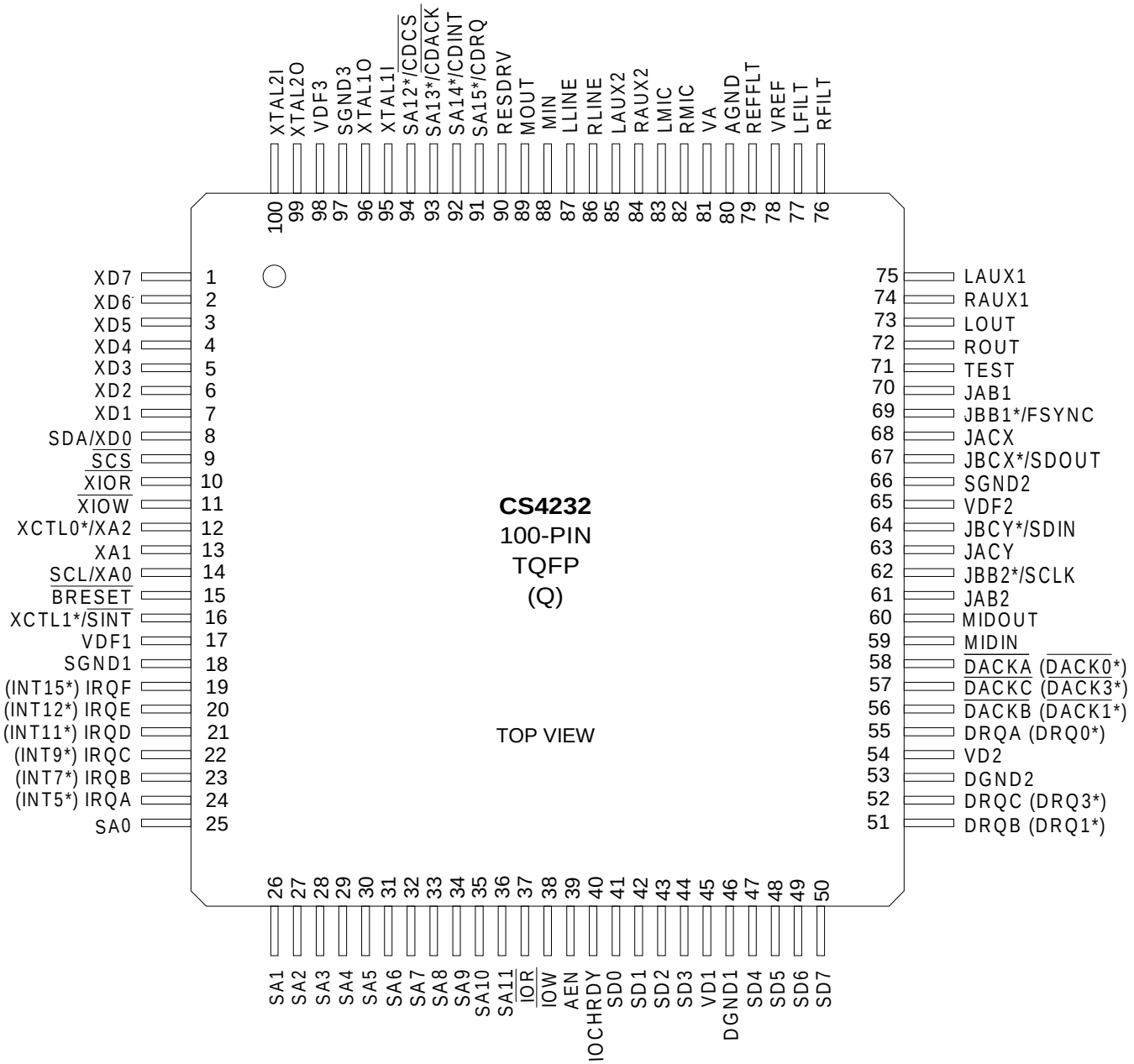


Figure 32. DAC Phase Response

PIN DESCRIPTIONS



*** Defaults** - Cannot be changed



*** Defaults** - See individual pin descriptions for more details

ISA Bus Interface Pins

SA<11:0> - System Address Bus, Inputs

These signals are decoded during I/O cycles to determine access to the various functional blocks within the CS4232 as defined by the configuration data written during a Plug And Play configuration sequence.

SA<15:12> - Upper System Address Bus, Inputs

These signals are dual function pins, shared with the CDROM interface, that default to the upper address bits SA12 through SA15. These pins are generally used for motherboard designs that want to eliminate address decode aliasing. Using these pins as upper address bits forces the CS4232 to only accept valid address decodes when A12-A15 = 0. If these pins are not used for address decodes (or for CDROM support), they should be tied to SGND.

SD<7:0> - System Data Bus, Bi-directional, 24mA drive

These signals are used to transfer data to and from the CS4232 and associated peripheral devices.

AEN - Address Enable, Input

This signal indicates whether the current bus cycle is an I/O cycle or a DMA cycle. This signal is low during an I/O cycle and high during a DMA cycle.

$\overline{\text{IOR}}$ - Read Command Strobe, Input

This active low signal defines a read cycle to the CS4232. The cycle may be a register read or a read from the CS4232 DMA registers.

$\overline{\text{IOW}}$ - Write Command Strobe, Input

This active low signal indicates a write cycle to the CS4232. The cycle may be a write to a control register or a CS4232 DMA register.

IOCHRDY - I/O Channel Ready, Open Drain Output, 8mA drive

This signal is driven low by the CS4232 during ISA bus cycles in which the CS4232 is not able to respond within a minimum cycle time. IOCHRDY is forced low to extend the current bus cycle. The bus cycle is extended until IOCHRDY is brought high.

DRQ<A,B,C> - DMA Requests, Outputs, 24mA drive

These active high outputs are generated when the CS4232 is requesting a DMA transfer. This signal remains high until all the bytes have been transferred as defined by the current transfer data type. The DRQ<A,B,C> outputs must be connected to 8-bit DMA channel request signals only. The defaults on the ISA bus are DRQA = DRQ0, DRQB = DRQ1, and DRQC = DRQ3. The defaults cannot be changed. If all the defaults are not used and the design supports Plug and Play, the Plug and Play resource data MUST be modified.

$\overline{\text{DACK}}$<A,B,C> - DMA Acknowledge, Inputs

The assertion of these active low signals indicate that the current DMA request is being acknowledged and the CS4232 will respond by either latching the data present on the data bus (write) or putting data on the bus (read). The $\overline{\text{DACK}}$<A,B,C> inputs must be connected to 8-bit DMA channel acknowledge lines only. The defaults on the ISA bus are $\overline{\text{DACKA}}$ = $\overline{\text{DACK0}}$, $\overline{\text{DACKB}}$ = $\overline{\text{DACK1}}$, and $\overline{\text{DACKC}}$ = $\overline{\text{DACK3}}$. The defaults cannot be changed. If all the defaults are not used and the design supports Plug and Play, the Plug and Play resource data MUST be modified.

IRQ <A:F>- Host Interrupt Pins, Outputs, 24mA drive

These signals are used to notify the host of events which need servicing. They are connected to specific interrupt lines on the ISA bus. The IRQ<A:F> are individually enabled as per configuration data that is generated during a Plug and Play configuration sequence. The defaults on the ISA bus are IRQA = INT5, IRQB = INT7, IRQC = INT9, IRQD = INT11, IRQE = INT12, IRQF = INT15. The defaults cannot be changed. If all the defaults are not used and the design supports Plug and Play, the Plug and Play resource data MUST be modified.

Analog Inputs

LLINE - Left Line Input

Nominally 1 V_{RMS} max analog input for the Left LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I0). A programmable gain block (I18) also allows routing to the mixer. Typically used for Left Channel Synthesis (FM or Wave Table).

RLINE - Right Line Input

Nominally 1 V_{RMS} max analog input for the Right LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I19) also allows routing to the mixer. Typically used for Right Channel Synthesis (FM or Wave Table).

LMIC - Left Mic Input

Microphone input for the Left MIC channel, centered around VREF. Full scale can be either 1 V_{RMS} (LMGE = 0) or 0.1 V_{RMS} (LMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I0).

RMIC - Right Mic Input

Microphone input for the Right MIC channel, centered around VREF. Full scale can be either 1 V_{RMS} (RMGE = 0) or 0.1 V_{RMS} (RMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I1).

LAUX1 - Left Auxiliary #1 Input

Nominally 1 V_{RMS} max analog input for the Left AUX1 channel, centered around VREF. The AUX1 input may be selected for A/D conversion via the input multiplexer (I0). A programmable gain block (I2) also allows routing to the output mixer. Typically used for an external Left line-level input.

RAUX1 - Right Auxiliary #1 Input

Nominally 1 V_{RMS} max analog input for the Right AUX1 channel, centered around VREF. The AUX1 input may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I3) also allows routing to the output mixer. Typically used for an external Right line-level input.

LAUX2 - Left Auxiliary #2 Input

Nominally 1 V_{RMS} max analog input for the Left AUX2 channel, centered around VREF. A programmable gain block (I4) also allows routing of the AUX2 channels into the output mixer. Typically used for the Left channel CDROM input.

RAUX1 - Right Auxiliary #1 Input

Nominally 1 V_{RMS} max analog input for the Right AUX2 channel, centered around VREF. A programmable gain block (I5) also allows routing of the AUX2 channels into the output mixer. Typically used for the Right channel CDROM input.

MIN - Mono Input

Nominally 1 V_{RMS} max analog input, centered around VREF, that goes through a programmable gain stage (I26) into both channels of the mixer. This is a general purpose mono analog input that is normally used to mix the typical "beeper" signal on most computers into the audio system

Analog Outputs

LOUT - Left Line Level Output

Analog output from the mixer for the left channel. Nominally 1 V_{RMS} max centered around VREF. This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

ROUT - Right Line Level Output

Analog output from the mixer for the Right channel. Nominally 1 V_{RMS} max centered around VREF. This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

MOUT - Mono Output

MOUT is nominally 1 V_{RMS} max analog output, centered around VREF. This output is a summed analog output from both the left and right output channels of the mixer. MOUT typically is connected to a speaker driver that drives the internal speaker in most computers. Independently mutable via MOM in I26.

MIDI Interface

MIDOUT - MIDI Out Transmit Data, Output, 4mA drive

This output is used to send MIDI data serially out to a external MIDI device. Normally connected to pin 12 of the joystick connector for use with breakout boxes.

MIDIN - MIDI In Receive Data, Input

This input is used to receive serial MIDI data from an external MIDI device. This pin should have a 47 kΩ pullup attached and is normally connected to pin 15 of the joystick connector for use with breakout boxes.

Synthesizer Interface

$\overline{\text{SCS}}$ - Synthesizer Chip Select, Output, 4 mA drive

This active low output is forced low when a valid address decode to the synthesizer , as defined in the Plug and Play configuration registers, has occurred.

XCTL1/$\overline{\text{SINT}}$ - XCTL1 or Synthesizer Interrupt, Output/Input

This pin defaults to the XCTL1 output which is controlled by the XCTL1 bit in the CS4232 register I10. This pin can be changed to $\overline{\text{SINT}}$ input by connecting a 10kΩ resistor between the $\overline{\text{XIOW}}$ pin and SGND. $\overline{\text{SINT}}$ is an active low input that should be driven by the synthesizer interrupt output pin.

External Peripheral Port

XD<7:1> - External Data Bus bits 7 through 1, Bi-directional, 4mA drive

These pins are used to transfer data between the ISA bus and external devices such as the synthesizer and CDROM.

SDA/XD0 - External Data Bus bit 0 and E^2PROM Data Pin, Bi-directional, Open Drain,4mA sink

This open-drain pin must have an external pullup (10kΩ) and is used to transfer data between the ISA bus bit 0, SD0, and external devices such as the synthesizer and CDROM. SDA/XD0 is also used in conjunction with SCL/XA0 to access an external serial E^2PROM. When an E^2PROM is used, the SDA/XD0 pin should be connected to the data pin of the E^2PROM device and provides a bi-directional data port. The E^2PROM is used to modify the default Plug and Play resource data.

XCTL0/XA2 - XCTL0 or External Address SA2, Output, 4mA drive

This pin either outputs ISA bus address SA2 or XCTL0 depending on the Plug-and-Play resource data. The default is XCTL0 which is controlled by the XCTL0 bit in the CS4232 register I10. This pin changes to address bit XA2 if the externally-loaded Plug-and-Play resource data indicates that the synthesizer or CDROM requires more than four I/O addresses.

XA1 - External Address, Output, 4mA drive

This pin outputs ISA bus address SA1.

XA0/SCL - External Address, Output/Serial Clock, Output, 4mA drive

This pin outputs the ISA bus address SA0. When E^2PROM access is enabled, then SCL is used as a clock output to the E^2PROM.

$\overline{\text{BRESET}}$ - Buffered Reset, Output, 4mA drive

This active low signal goes low whenever the RESDRV pin goes high.

$\overline{\text{XIOR}}$ - External Read Strobe, Output, 4mA drive (SA12-SA15/CDROM selection)

This active low signal goes low whenever ($\overline{\text{SCS}}$ or $\overline{\text{CDCS}}$) and $\overline{\text{IOR}}$ goes low. This pin also selects either the CDROM port or SA12 - SA15 and contains an internal pullup of approximately 100 kΩ. The selection is made when RESDRV goes low. When $\overline{\text{XIOR}}$ is left high (default), pins 91-94 are SA15-SA12 respectively. To enable the CDROM port, an external 10kΩ resistor must be tied between this pin and SGND.

$\overline{\text{XIOW}}$ - External Write Strobe, Output, 4mA drive (XCTL1/$\overline{\text{SINT}}$ selection)

This active low signal goes low whenever ($\overline{\text{SCS}}$ or $\overline{\text{CDCS}}$) and $\overline{\text{IOW}}$ goes low. This pin also selects either XCTL1 or $\overline{\text{SINT}}$ and contains an internal pullup of approximately 100 kΩ. The selection is made when RESDRV goes low. When $\overline{\text{XIOW}}$ is left high (default), pin 16 is the XCTL1 function. To change the pin to $\overline{\text{SINT}}$, an external 10kΩ resistor must be tied between this pin and SGND.

Joystick/Serial Port Interface

JACX, JACY - Joystick A Coordinates, Input

These pins and are the X/Y coordinates for Joystick A. They should have a 5.6nF capacitor to ground and a 2.2kΩ resistor to the joystick connector pins 3 and 6, respectively.

JAB1, JAB2 - Joystick A Buttons, Input

These pins are the switch inputs for Joystick A. They should be connected to joystick connector pins 2 and 7, respectively; as well as have a 1nF capacitor to ground, and a 4.7kΩ pullup resistor.

JBCX/SDOUT - Joystick B Coordinate X/Serial Data Output, Input/Output

When this pin is used as a second joystick, it is the X coordinates input for Joystick B; and should have a 5.6nF capacitor to ground and a 2.2kΩ resistor to the joystick connector pin 11. When the serial port is enabled, SPE = 1 in I16, this pin is the serial data output. It should have a 5.6nF capacitor to ground and a 2.2kΩ resistor to the joystick connector pin 11.

JBCY/SDIN - Joystick B Coordinate Y/Serial Data Input, Input

When this pin is used as a second joystick, it is the Y coordinates input for Joystick B; and should have a 5.6nF capacitor to ground and a 2.2kΩ resistor to the joystick connector pin 13. When the serial port is enabled, SPE = 1 in I16, this pin is the serial data input.

JBB1/FSYNC - Joystick B Button 1/Frame Sync, Input/Output

When this pin is used as a second joystick, it is the switch 1 input for Joystick B; and should be connected to joystick connector pin 10; as well as have a 1nF capacitor to ground, and a 4.7kΩ pullup resistor. When the serial port is enabled, SPE = 1 in I16, this pin is the serial frame sync output.

JBB2/SCLK - Joystick B Button 2/Serial Clock, Input/Output

When this pin is used as a second joystick, it is the switch 2 input for Joystick B; and should be connected to joystick connector pin 14; as well as have a 1nF capacitor to ground, and a 4.7kΩ pullup resistor. When the serial port is enabled, SPE = 1 in I16, this pin is the serial clock output.

CDROM Interface

The four CDROM pins are dual function and default to ISA upper address bits SA12-SA15. To enable the CDROM port, an external 10kΩ resistor must be tied between $\overline{\text{XIOR}}$ and SGND. $\overline{\text{XIOR}}$ is sampled on the falling edge of RESDRV.

$\overline{\text{CDCS}}$ - CDROM Chip Select, Output, 4mA drive

This output is goes low whenever the CS4232 decodes an address that matches the value programmed into the CDROM base address register.

$\overline{\text{CDACK}}$ - CDROM DMA Acknowledge, Output, 4mA drive

This pin is used to output the ISA bus-generated DMA acknowledge signal to the CDROM interface.

CDINT - CDROM Interrupt, Input

This pin is used to input an interrupt signal from the CDROM interface. The CS4232 can be programmed, through the plug-and-play resource data, to output this signal to the appropriate ISA bus interrupt line.

CDRQ - CDROM DMA Request, Input

This pin is used to input the DMA request signal from the CDROM interface. The CS4232 can be programmed, through the plug-and-play resource data, to output this signal to the appropriate ISA bus DRQ line.

Miscellaneous

XTAL1I - Crystal #1 Input

This pin will accept either a crystal, with the other pin attached to XTAL1O, or an external CMOS clock. XTAL1 must have a crystal or clock source attached for proper operation. The standard crystal frequency is 24.576 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL1O - Crystal #1 Output

This pin is used for a crystal placed between this pin and XTAL1I.

XTAL2I - Crystal #2 Input

This pin will accept either a crystal, with the other pin attached to XTAL2O, or an external CMOS clock. XTAL2 must have a crystal or clock source attached for proper operation. The standard crystal frequency is 16.9344 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL2O - Crystal #2 Output

This pin is used for a crystal placed between this pin and XTAL2I.

RESDRV - Reset Drive, Input

Places CS4232 in lowest power consumption mode. All sections of the CS4232, except the digital bus interface, which reads 80h, are shut down and consuming minimal power. The CS4232 is reset and in power down mode when this pin is logic high. The falling edge also latches the state of $\overline{\text{XIOR}}$ and $\overline{\text{XIOW}}$ to determine the functionality of dual mode pins. This signal is typically connected to the ISA bus signal RESDRV.

VREF - Voltage Reference, Output

All analog inputs and outputs are centered around VREF which is nominally 2.1 Volts. This pin may be used to level shift external circuitry, although any AC loads should be buffered. High internal-gain microphone inputs can be slightly improved by placing a 10µF capacitor on VREF.

REFFLT - Reference Filter, Input

Voltage reference used internal to the CS4232. A 0.1 µF and a 10 µF capacitor with short fat traces must be connected to this pin. No other connections should be made to this pin.

LFILT - Left Channel Antialias Filter Input

This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

RFILT - Right Channel Antialias Filter Input

This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

TEST - Test

This pin must be tied to ground for proper operation.

Power Supplies

VA - Analog Supply Voltage

Supply to the analog section of the codec.

AGND - Analog Ground

Ground reference to the analog section of the codec. Internally, this pin is connected to the substrate as are all SGND pins; therefore, optimum layout is achieved with the AGND pin on the same ground plane as SGND1/2/3 (see Figure 25).

VD1, VD2 - Digital Supply Voltage

Digital supply for the parallel data bus section of the codec.

DGND1, DGND2 - Digital Ground

Digital ground reference for the parallel data bus section of the codec. These pins are isolated from the other grounds and should be connected to the digital ground section of the board (see Figure 25).

VDF1, VDF2, VDF3 - Digital Filtered Supply Voltage

Digital supply for the internal digital section of the codec (except for the parallel data bus). These pins should be filtered, using a ferrite bead, from VD1/VD2.

SGND1, SGND2, SGND3 - Substrate Ground

Substrate ground reference for the codec . These pins are connected to the substrate of the die as is the AGND pin. Optimum layout is achieved by placing SGND1/2/3 on the analog ground plane with the AGND pin as shown in Figure 25.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e. attenuation bits for the DACs at full attenuation). Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

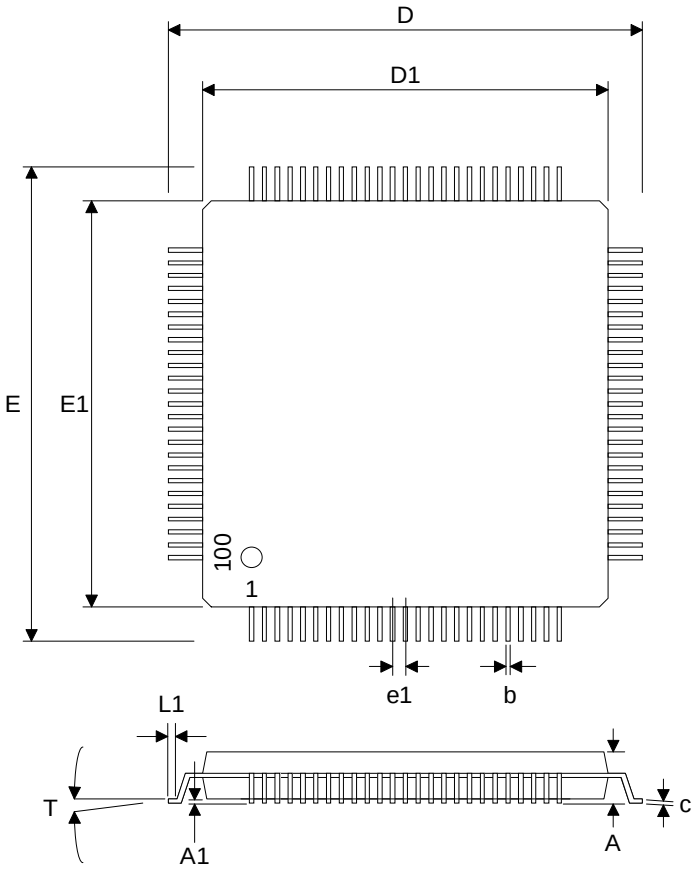
Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation in volts of the output from VREF with mid-scale input code.

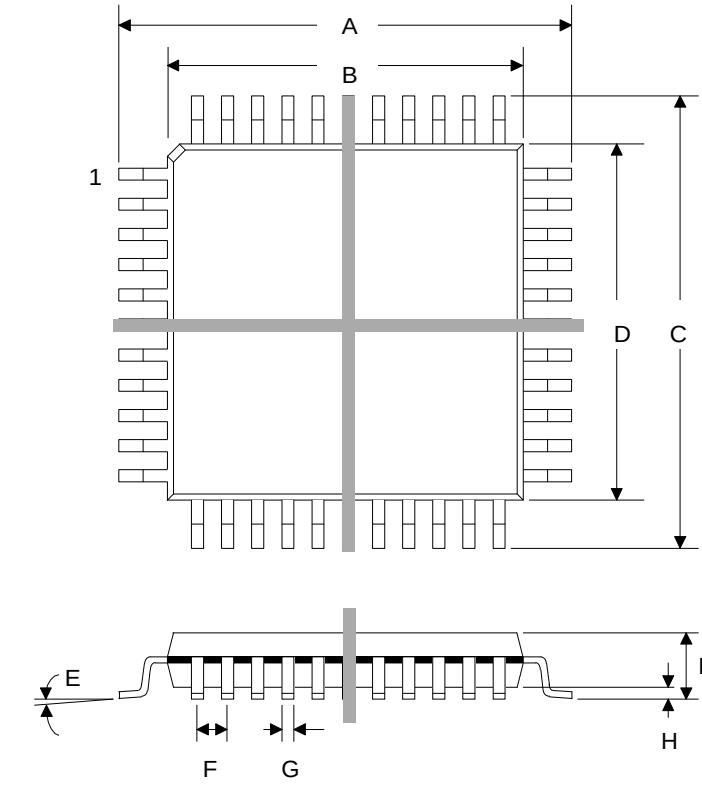
PACKAGE PARAMETERS



100-pin TQFP - Package Code 'Q'

Symbol	Description	MIN	NOM	MAX
N	Lead Count		100	
A	Overall Height			1.66
A1	Stand Off	0.00		
b	Lead Width	0.14	0.20	0.26
c	Lead Thickness	0.077	0.127	0.177
D	Terminal Dimension	15.70	16.00	16.30
D1	Package Body		14.0	
E	Terminal Dimension	15.70	16.00	16.30
E1	Package Body		14.0	
e1	Lead Pitch	0.40	0.50	0.60
L1	Foot Length	0.30	0.50	0.70
T	Lead Angle	0.0°		12.0°

Notes:
1) Dimensions in millimeters.
2) Package body dimensions do not include mold protrusion, which is 0.25 mm.
3) Coplanarity is 0.004 in.
4) Lead frame material is AL-42 or copper, and lead finish is solder plate.
5) Pin 1 identification may be either ink dot or dimple.
6) Package top dimensions can be smaller than bottom dimensions by 0.20 mm.
7) The "lead width with plating" dimension does not include a total allowable dambar protrusion of 0.08 mm (at maximum material condition).
8) Ejector pin marks in molding are present on every package.



100-Pin PQFP (Rectangular)
Package Code 'M'

	MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**
A	16.95	17.20	17.45
B		14.0	
C	22.95	23.20	23.45
D		20.0	
E	0 o		10 o
F	0.53	0.65	0.77
G	0.20	0.30	0.40
H	0.00		
I			3.15
J	0.65	0.80	0.95
K	0.10	0.15	0.20

Plastic QUAD FLATPACK

APPENDIX A: TYPICAL E^{2}PROM DATA

```
; EEPROM Validation Bytes
  DB       055H, 0AAH                ; EEPROM Validation Bytes

  DB       000H                       ; EEPROM data length upper byte
  DB       0F5H                       ; lower byte, Listed Size = 245

; Hardware Configuration Data (Resource Header)
  DB       000H                       ; 00=4/08=8 peripheral port size, XCTL0/XA2
  DB       048H                       ; LINE, AUX1, AUX2 mapping - RESERVED
  DB       075H                       ; IRQ selection A & B - B= 7,   A=5
  DB       0B9H                       ; IRQ selection C & D - D=11,   C=9
  DB       0FCH                       ; IRQ selection E & F - F=15,   E=12
  DB       010H                       ; DMA selection A & B - B= 1,   A=0
  DB       003H                       ; DMA selection C      -          C=3

; PnP Resource Header - Starts with Crystal PnP ID for CS4232 IC
  DB       00EH, 063H, 042H, 032H, 001H,000H,000H,000H,0D3H  ; CSC4232 00000001
  DB       00AH, 010H, 001H          ; PnP version 1.0, Vendor version 0.1
  DB       082H, 007H, 000H, 'CS4232', 000H ; ANSI ID

; LOGICAL DEVICE 0 (Windows Sound System & OPL3 & SBPro)
  DB       015H, 00EH, 063H, 000H, 000H, 000H ; EISA ID: CSC0000

  DB       082H, 00BH, 000H, 'WSS/OPL/SB', 000H ; ANSI ID
  DB       031H, 000H                 ; DF Best Choice
  DB       02AH, 002H, 028H          ; DMA: 1   - WSS & SBPro
  DB       02AH, 009H, 028H          ; DMA: 0,3   - WSS & SBPro capture
  DB       022H, 020H, 000H          ; IRQ: 5  Interrupt Select 0
  DB       047H, 001H, 034H, 005H, 034H, 005H, 004H, 004H ; 16b WSSbase: 534
  DB       04BH, 088H, 003H, 004H   ; 10b SYNbase: 388
  DB       04BH, 020H, 002H, 010H   ; 10b SBbase: 220

  DB       031H, 001H                 ; DF Acceptable Choice 1
  DB       02AH, 00BH, 028H          ; DMA: 0,1,3   - WSS & SBPro
  DB       022H, 0A0H, 09AH          ; IRQ: 5,7,9,11,12,15  Interrupt Select 0
  DB       047H, 001H, 000H, 001H, 0FCH, 00FH, 004H, 004H ; 16b WSSbase: 100-FFC
  DB       047H, 000H, 000H, 001H, 0FCH, 003H, 004H, 004H ; 10b SYNbase: 100-3FC
  DB       047H, 000H, 000H, 001H, 0F0H, 003H, 010H, 010H ; 10b SBbase: 100-3F0

  DB       038H                       ; End of DF for Logical Device 0

  DB       01CH, 041H, 0D0H, 0B0H, 007H ; Compatible ID: PNPB007
  DB       01CH, 041H, 0D0H, 0B0H, 020H ; Compatible ID: PNPB020
  DB       01CH, 041H, 0D0H, 0B0H, 002H ; Compatible ID: PNPB002
```

```
; LOGICAL DEVICE 1 (Game Port)
  DB       015H, 00EH, 063H, 000H, 001H, 000H ; EISA ID: CSC0001

  DB       082H, 005H, 000H, 'GAME', 000H ; ANSI ID
  DB       031H, 000H                ; DF Best Choice
  DB       04BH, 000H, 002H, 008H  ; 10b GAMEbase: 200

  DB       031H, 001H                ; DF Acceptable Choice 1
  DB       047H, 000H, 000H, 001H, 0F8H, 003H, 008H, 008H ; 10b GAMEbase: 100-3F8

  DB       038H                       ; End of DF for Logical Device 1

  DB       01CH, 041H, 0D0H, 0B0H, 02FH ; Compatible ID: PNPB02F

; LOGICAL DEVICE 2 (Control)
  DB       015H, 00EH, 063H, 000H, 002H, 000H ; EISA ID: CSC0002

  DB       082H, 005H, 000H, 'CTRL', 000H ; ANSI ID
  DB       047H, 001H, 000H, 001H, 0F8H, 00FH, 008H, 008H ; 16b CTRLbase: 100-FF8

; LOGICAL DEVICE 3 (MPU-401)
  DB       015H, 00EH, 063H, 000H, 003H, 000H ; EISA ID: CSC0003

  DB       082H, 004H, 000H, 'MPU', 000H ; ANSI ID
  DB       031H, 000H                ; DF Best Choice
  DB       022H, 000H, 002H         ; IRQ: 9  Interrupt Select 0
  DB       04BH, 030H, 003H, 002H  ; 10b MPUbase: 330

  DB       031H, 001H                ; DF Acceptable Choice 1
  DB       022H, 0A0H, 09AH         ; IRQ: 5,7,9,11,12,15  Interrupt Select 0
  DB       047H, 000H, 000H, 001H, 0F8H, 003H, 008H, 002H ; 10b MPUbase: 100-3F8

  DB       038H                       ; End of DF for Logical Device 3

  DB       01CH, 041H, 0D0H, 0B0H, 006H ; Compatible ID: PNPB006

; LOGICAL DEVICE 4 (CD-ROM)
  DB       015H, 00EH, 063H, 000H, 004H, 000H ; EISA ID: CSC0004

  DB       082H, 003H, 000H, 'CD', 000H ; ANSI ID
  DB       047H, 000H, 000H, 001H, 0FCH, 003H, 004H, 004H ; 10b CDbase: 100-3FC

  DB       079H, 0A4H                ; End of Resource Data, Checksum
```

• Notes •